SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: Microcontroller Programming And Interfacing

Subcode:23ECB202

Unit-I

PIC Microcontrollers: History, Features, & Architecture

PIC16F877A Memory Organization

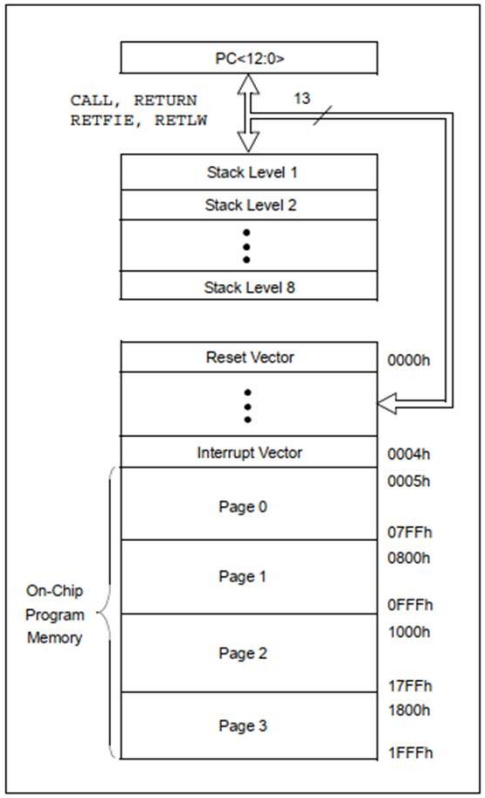
MEMORY ORGANIZATION

- There are three memory blocks in each of the PIC16F87XA devices.
- Program Memory
- Data Memory have separate buses so that concurrent access can occur and is detailed in this section.
- EEPROM data memory block

  Data EEPROM

  Flash Program Memory

Program Memory



- The PIC16F87XA devices have a 13-bit program counter capable of addressing an 8K word x 14 bit program memory space.
- The PIC16F876A/877A devices have 8K words x 14 bits of Flash program memory.
- Accessing a location above the physically implemented address will cause a wraparound.
- The Reset vector is at 0000h and the interrupt vector is at 0004h.

Data Memory Organization

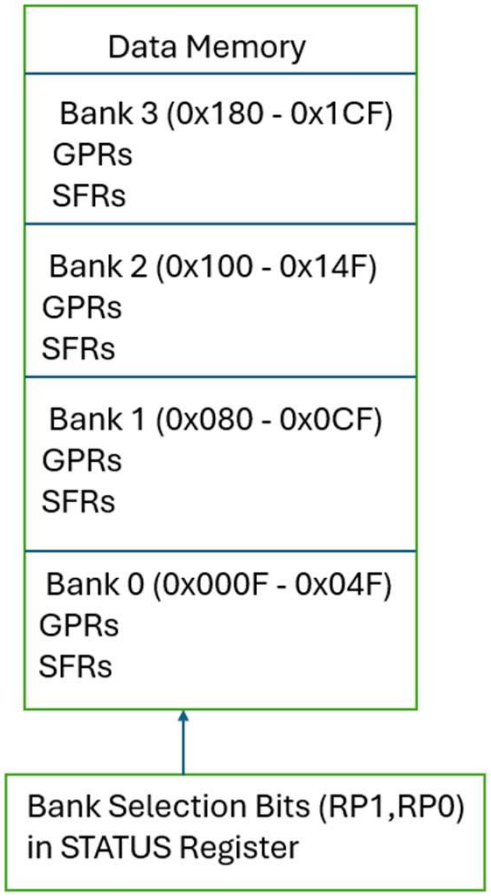
- The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers.
- Bits RP1 (Status<6>) and RP0 (Status<5>) are the bank select bits

RP1:RP0	Bank
00	0
01	1
10	2
11	3

- Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers.

Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers.

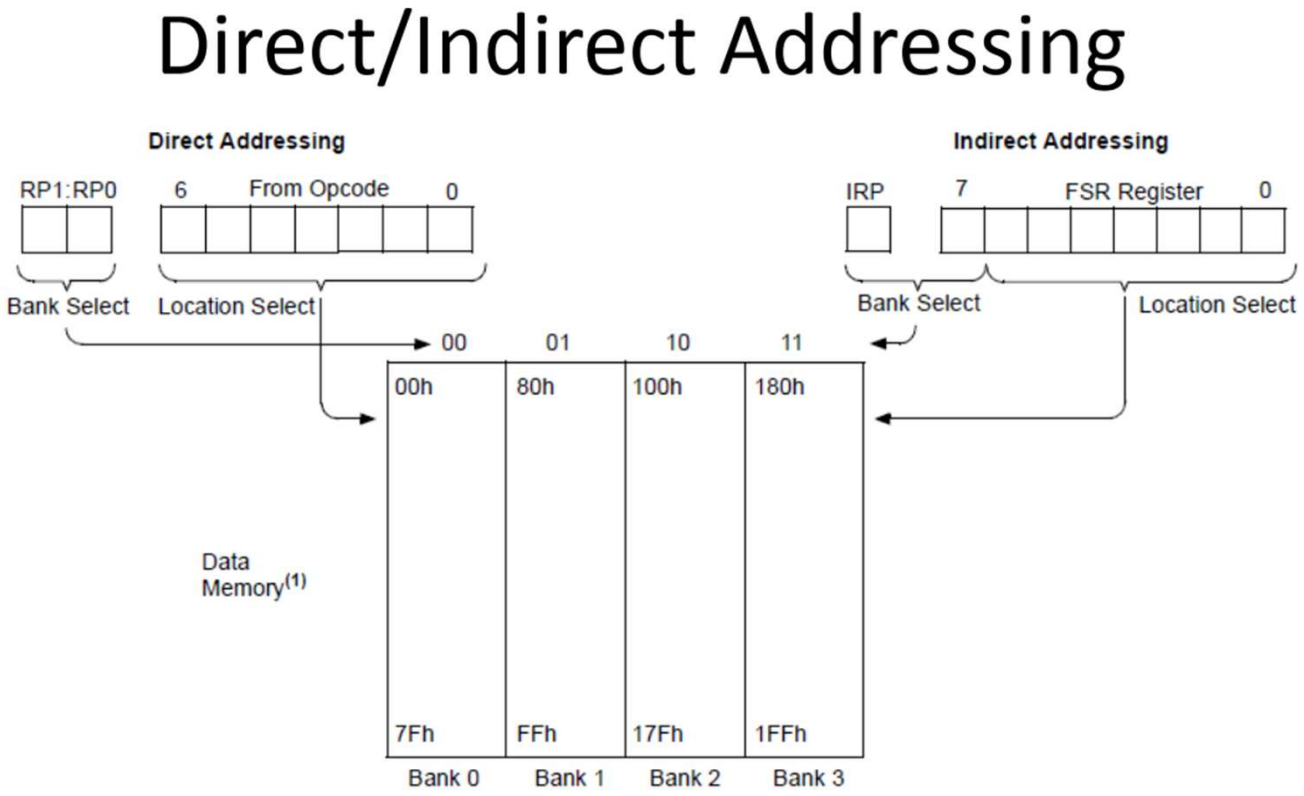
Data Memory Organization



This data memory region can be used for :

- Intermediate Computational Values
- Local variables of subroutines
- Faster context saving /switching of variables
- Common variables
- Faster Evaluation/control of SFR

Bank Selection using Direct and Indirect Addressing



EEPROM

The data EEPROM and Flash program memory is readable and writable during normal operation (over the full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1 – EEPROM Control Register 1 (used for memory access control)
- EECON2 – EEPROM Control Register 2 (used for write sequence control)
- EEDATA – EEPROM Data Register (holds the data to be read from or written to EEPROM)
- EEDATH – EEPROM Data Register High (upper byte of EEPROM data)
- EEADR – EEPROM Address Register (holds the address of the EEPROM location to access)
- EEADRH – EEPROM Address Register High (upper byte of EEPROM address for larger memory access)