SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: Microcontroller Programming And Interfacing

Subcode:23ECB202

Unit-I

PIC Microcontrollers: History, Features, & Architecture

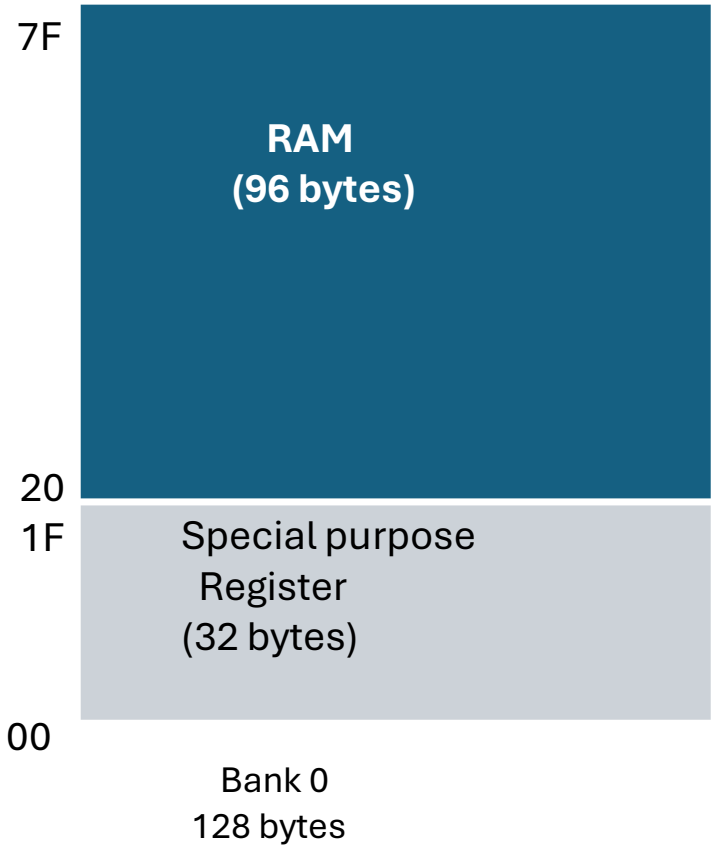
16F877a or16F8XX Registers File Structure

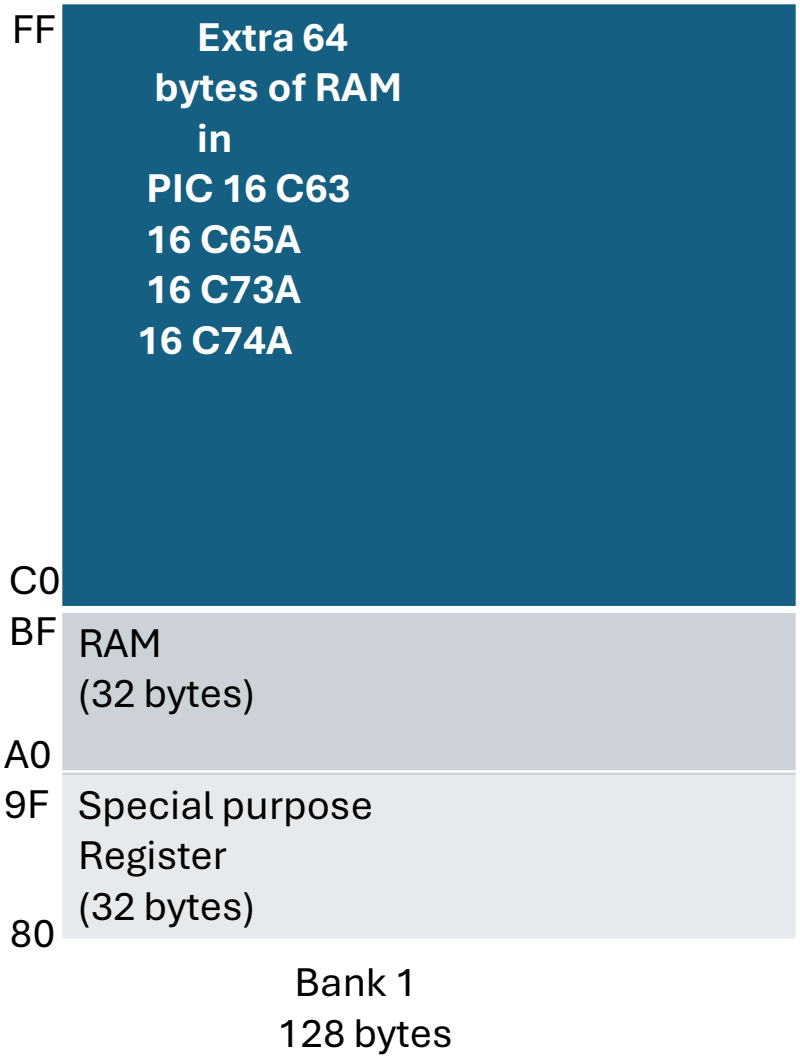
The Registers

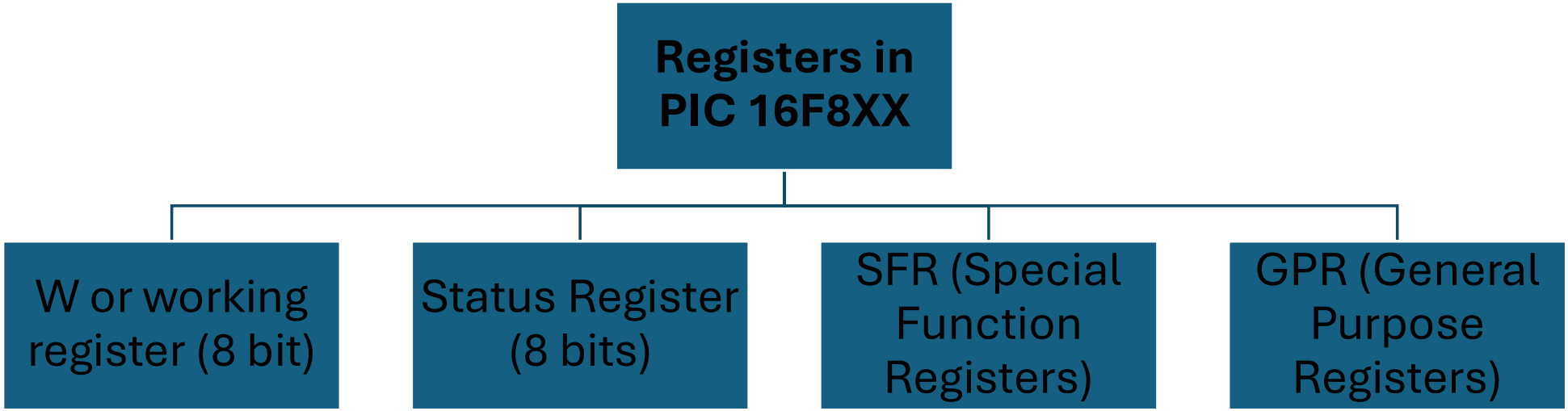
A register is a place inside the PIC that can be written to, read from or both. Think of a register as a piece of paper where you can look at and write information on.

Register File Structure

- Register file → *locations that an instruction can access via an address.*
- Register file consists of two component:-
    1. General purpose register file (same as RAM)
    2. Special purpose register file


7F
RAM
(96 bytes)
20
1F
Special purpose
Register
(32 bytes)
00
Bank 0
128 bytes


FF
Extra 64
bytes of RAM
in
PIC 16 C63
16 C65A
16 C73A
16 C74A
C0
BF
RAM
(32 bytes)
A0
9F
Special purpose
Register
(32 bytes)
80
Bank 1
128 bytes


Registers in PIC 16F8XX
W or working register (8 bit)
Status Register (8 bits)
SFR (Special Function Registers)
GPR (General Purpose Registers)

W or Working Register

- 8 bits wide
- Contains one of the source operands during the execution of instructions.
- Serve as the destination for the result of the operation.
- Only used for ALU operations..

Status Register (8 bits)

	R/W (0)	R/W (0)	R/W (0)	R (1)	R (1)	R/W (x)	R/W (x)	R/W (x)	Features
STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

IRP - Bit selects register bank. It is used for indirect addressing.	• 1 - Banks 0 and 1 are active (memory location 00h-FFh) • 0 - Banks 2 and 3 are active (memory location 100h-1FFh)
RP1,RP0	• Bits select register bank. They are used for direct addressing.
TO - Time-out bit.	• 1 - After power-on or after executing CLRWDT instruction which resets watch-dog timer or SLEEP instruction which sets the microcontroller into low-consumption mode. • 0 - After watch-dog timer time-out has occurred.
PD - Power-down bit.	• 1 - After power-on or after executing CLRWDT instruction which resets watch-dog timer. • 0 - After executing SLEEP instruction which sets the microcontroller into low-consumption mode.
Z - Zero bit	• 1 - The result of an arithmetic or logic operation is zero. • 0 - The result of an arithmetic or logic operation is different from zero.
DC - Digit carry/borrow bit is changed during addition and subtraction if an "overflow" or a "borrow" of the result occurs.	• 1 - A carry-out from the 4th low-order bit of the result has occurred. • 0 - No carry-out from the 4th low-order bit of the result has occurred.
C - Carry/Borrow bit is changed during addition and subtraction if an "overflow" or a "borrow" of the result occurs, i.e. if the result is greater than 255 or less than 0.	• 1 - A carry-out from the most significant bit of the result has occurred. • 0 - No carry-out from the most significant bit of the result has occurred.

- Microchip has provided only direct addressing mode for the register file with 7-bits address plus remaining 8th and 9th bits frozen in the STATUS REGISTER bits RP1:RP0.

11 = Bank 3 (180h-1FFh)

10 = Bank 2 (100h-17Fh)

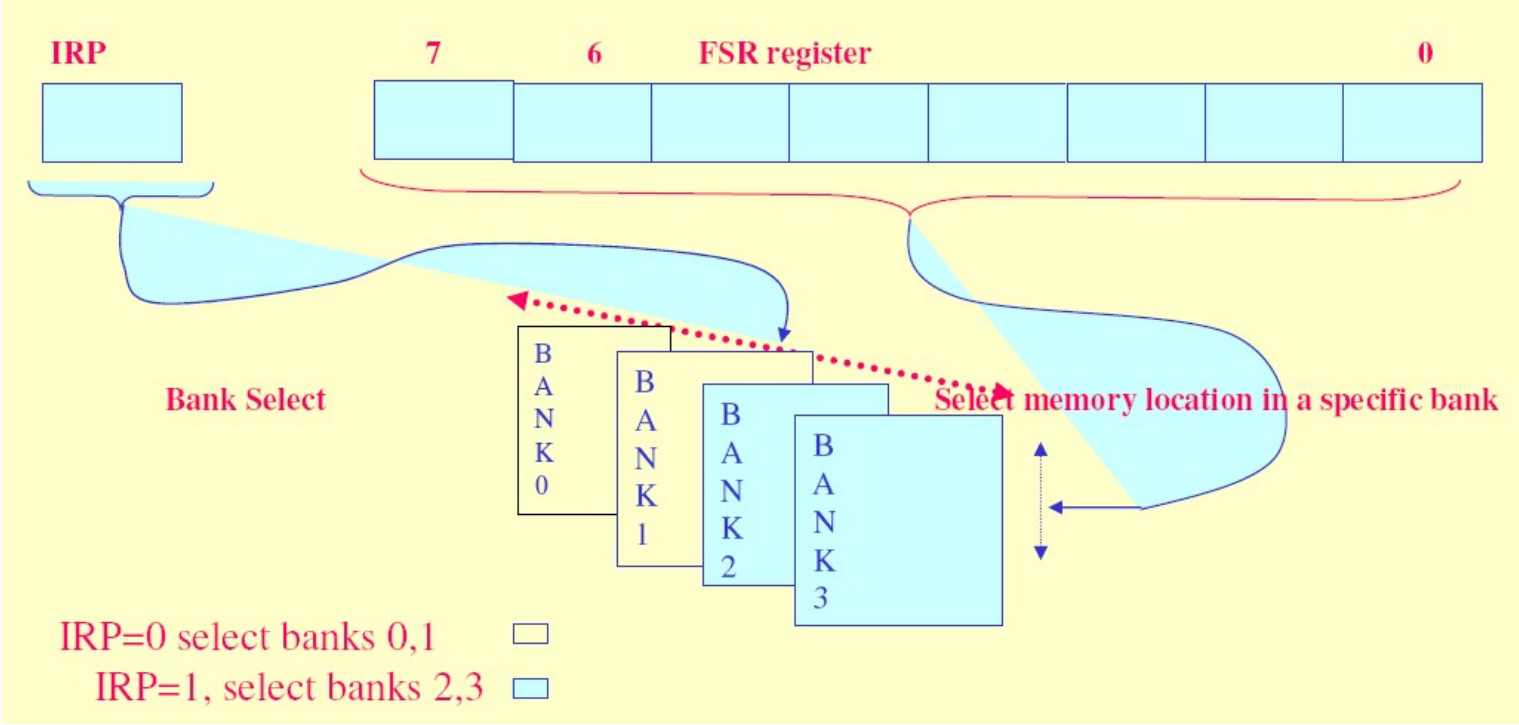
01 = Bank 1 (80h-FFh)

00 = Bank 0 (00h-7Fh)

As shown in figure

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Use of IPR bit in indirect addressing mode

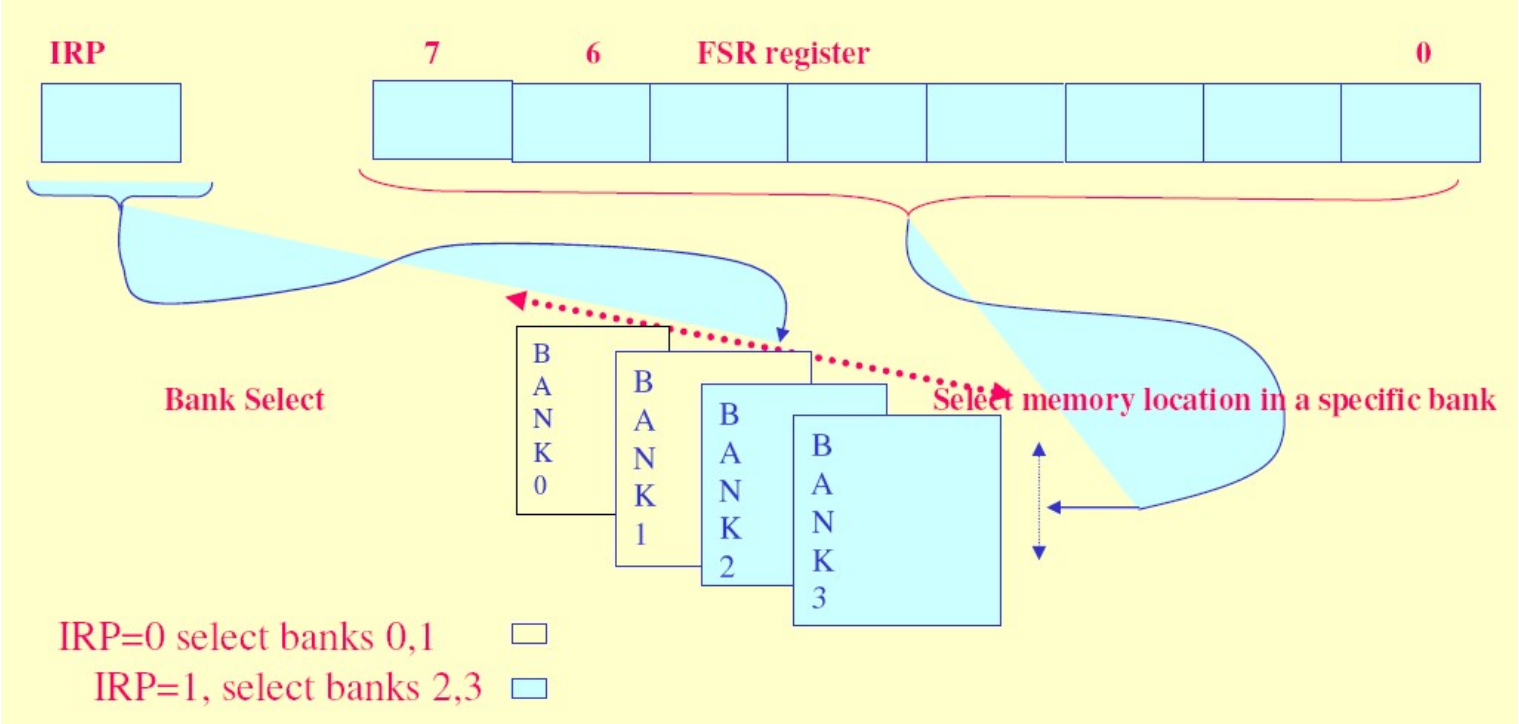


Indirect addressing mode

- IRP bit is used for indirect addressing.
- The IRP bit allows selecting either
  1= Bank 2 & bank 3
  0= Bank 0 & bank 1
- The IPR bit and FSR decide the effective 9 bit address.

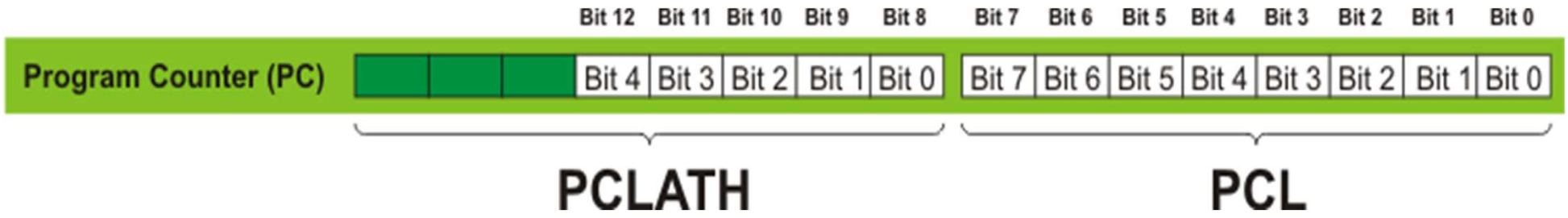
As shown in figure

Use of IPR bit in indirect addressing mode



Special Function Register

- **PCL and PCLATH Registers:** The size of the program memory of the PIC16F887 is 8K. Therefore, it has 8192 locations for program storing. For this reason the program counter must be 13-bits wide (2^13 = 8192). In order that the contents of some location may be changed in software during operation, its address must be accessible through some SFR. Since all SFRs are 8-bits wide, this register is “artificially” created by dividing its 13 bits into two independent registers: PCLATH and PCL.



- Eight lower bits (the low byte) come from the PCL register which is readable and writable, whereas five upper bits coming from the PCLATH register are writable only.

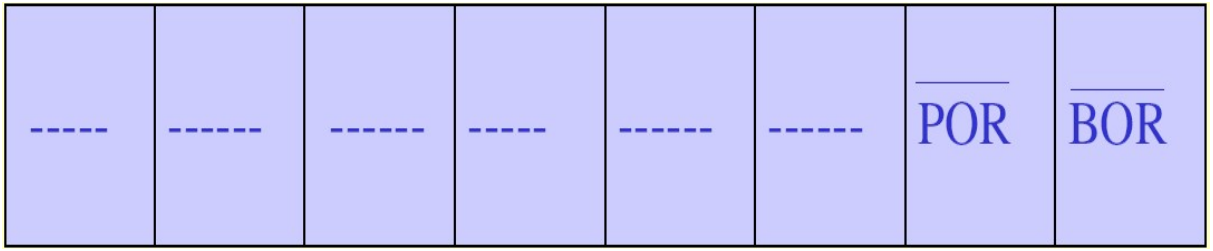
- The PCLATH register is cleared on any reset.

PCL

- Program Counter byte.
- PCL is the lower byte of the PC.
- Cause PCLATH contents to be transferred to the PC higher bit locations.
- PC of PIC is associated with an 8-level stack.
- PC always points to the next instruction to be executed.
- In case of call to subroutines, the returned address is pushed onto the stack.
- After the return from called subroutine, this return address is retrieved.
- Stack width and PC width should be same.

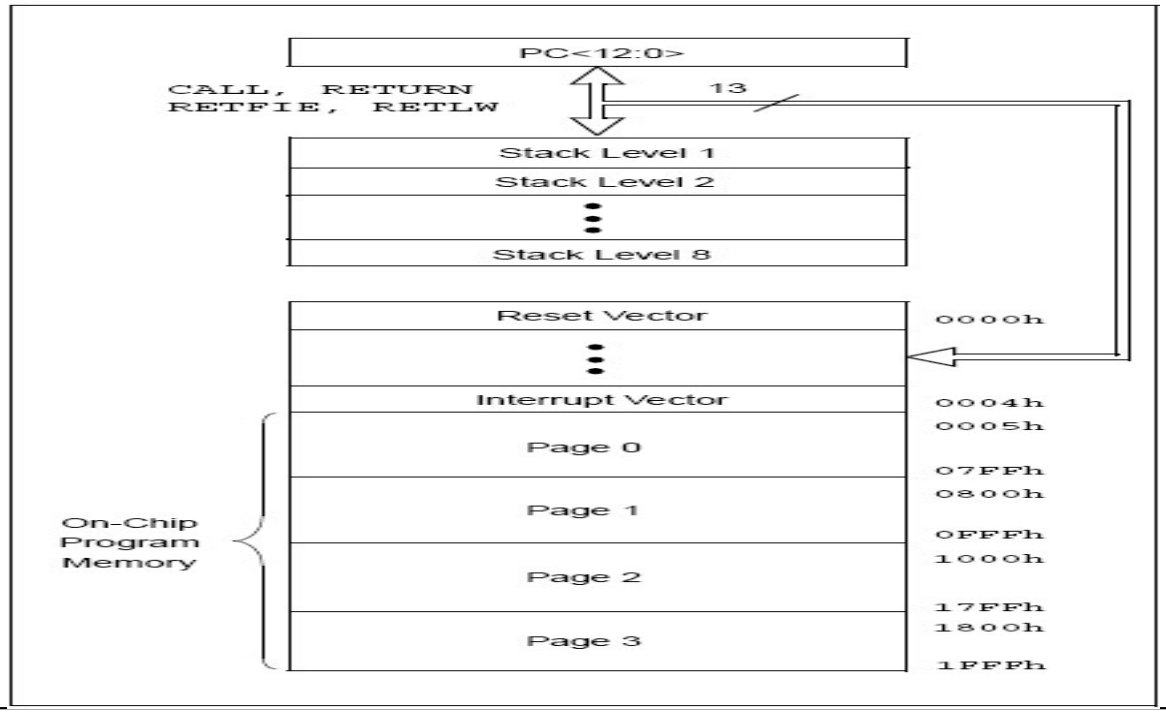
Power control register

- Contains the flags which can differentiate between the type of reset occurred namely
  - Power on reset
  - Brown out reset



Stack

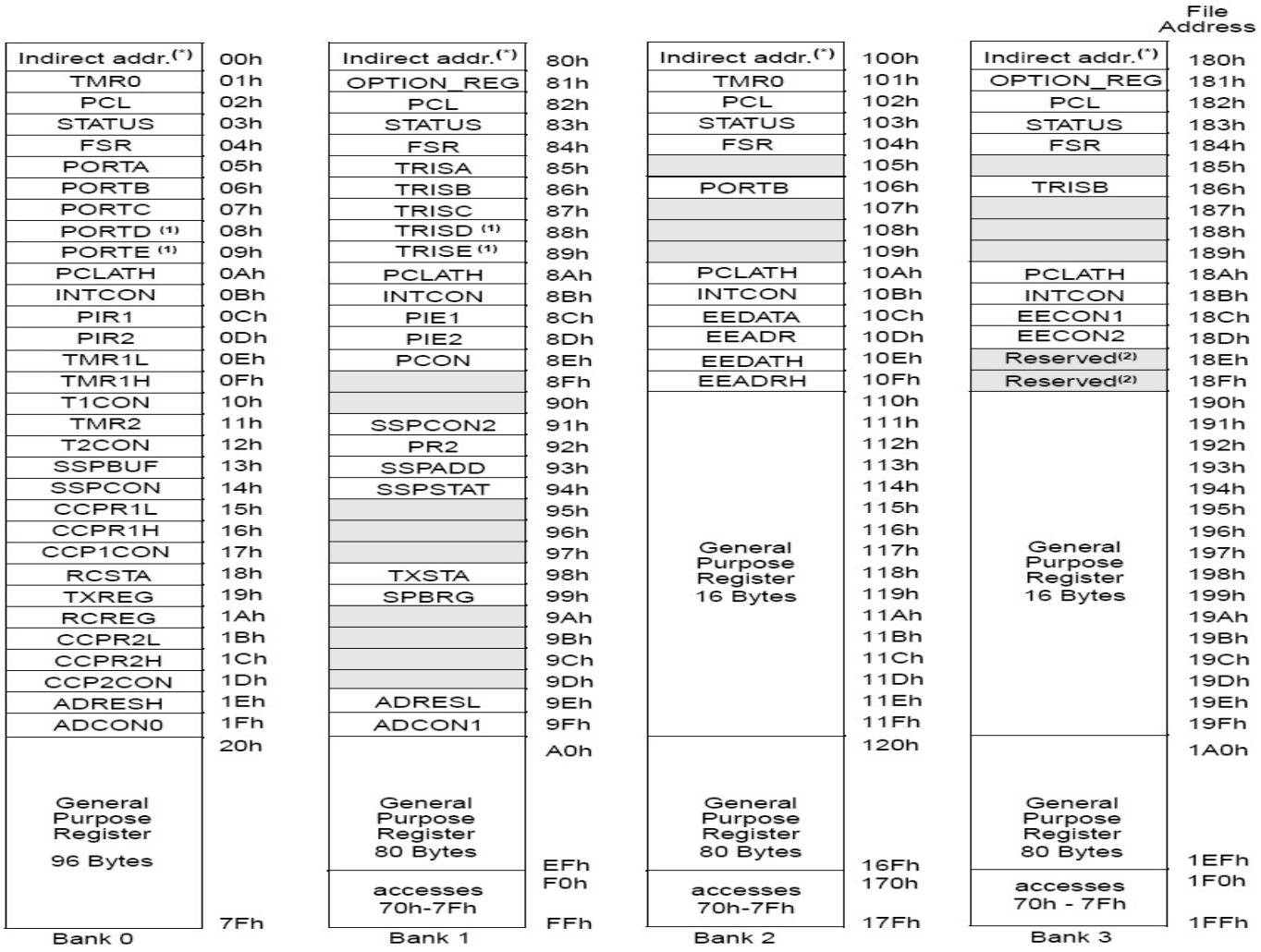
- The entire PIC chip has an area for storing the return addresses.
- This area or unit called Stack is used in some Peripheral interface controllers.



PIC16F87XA Data Memory Organization

- Data memory is divided in two four banks, Each bank holds 128 bytes of addressable memory.
- Contain GPR and SPR.
- The banked arrangement is necessary because there are only 7 bits are available in the instruction word for the addressing of a register, which gives only 128 addresses.
- The selection of the banks are determined by control bits RP1, RP0 in the STATUS registers
- Together the RP1, RP0 and the specified 7 bits effectively form a 9 bit address.

Register File Structure in PIC 16F8xx



Thanks