



# SNS COLLEGE OF ENGINEERING

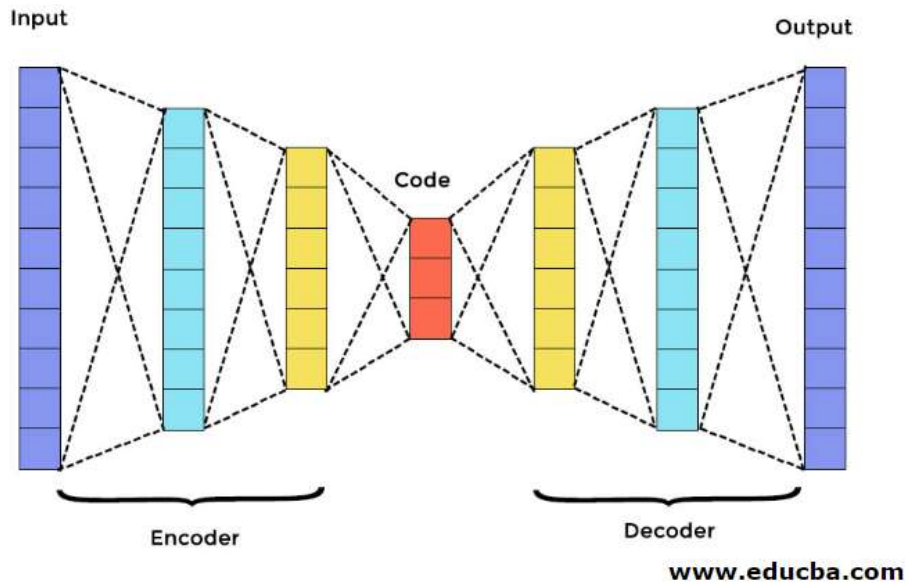
(Autonomous)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



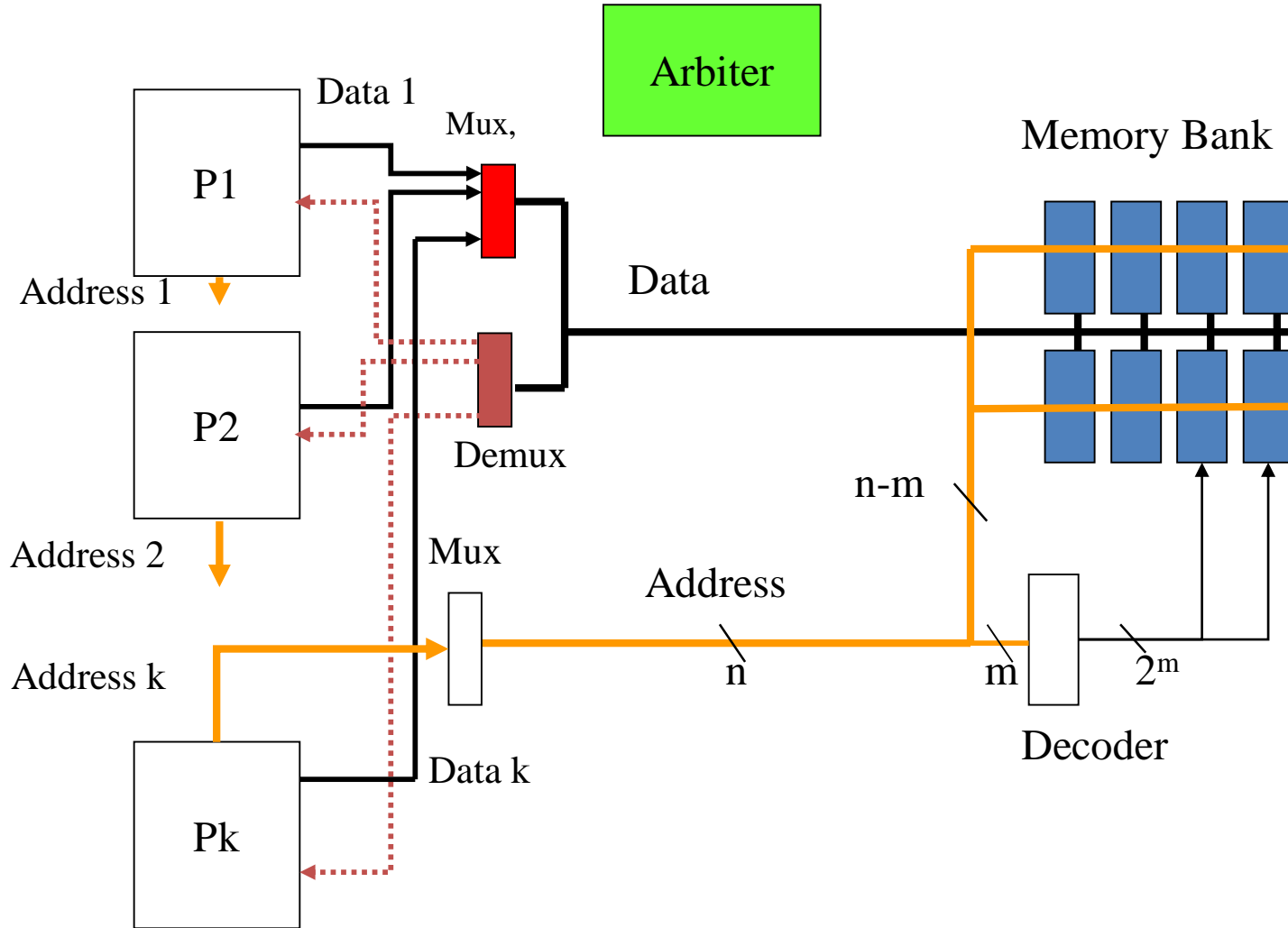
## 23ECB204 – DIGITAL ELECTRONICS AND MICROPROCESSOR

### UNIT -1 COMBINATIONAL LOGIC





# Interconnect: Decoder, Encoder, Mux, DeMux





# 1. Decoder

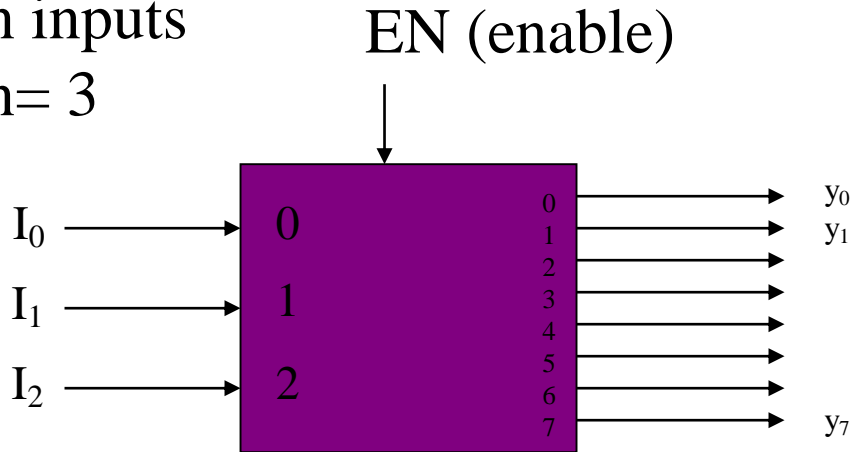
- Definition
- Logic Diagram
- Application (Universal Set)
- Tree of Decoders





# 1. Decoder: Definition

n inputs  
n= 3



$2^n$  outputs  
 $2^3 = 8$

n to  $2^n$  decoder  
function:

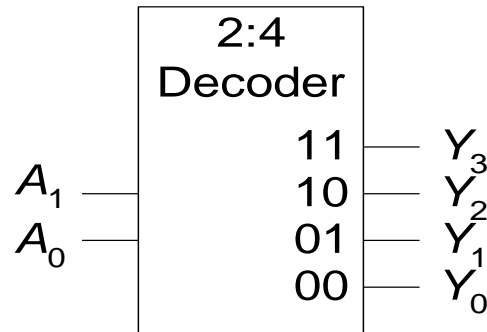
$$y_i = 1 \text{ if } E_n = 1 \text{ \& } (I_2, I_1, I_0) = i$$
$$y_i = 0 \text{ otherwise}$$





# 1. Decoder: Definition

- $N$  inputs,  $2^N$  outputs
- One-hot outputs: only one output HIGH at once

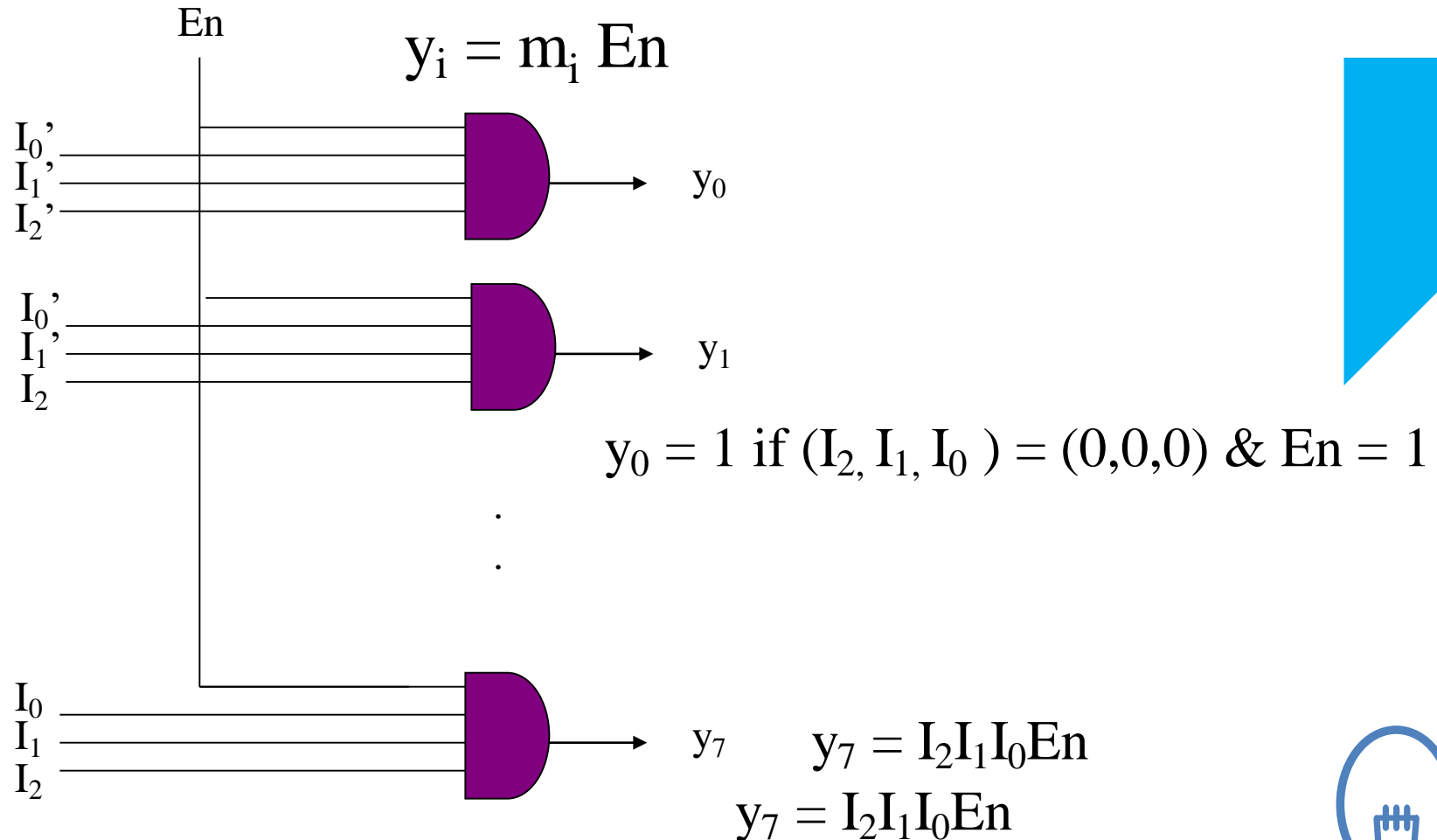


| $A_1$ | $A_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|-------|-------|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     | 0     | 1     |
| 0     | 1     | 0     | 0     | 1     | 0     |
| 1     | 0     | 0     | 1     | 0     | 0     |
| 1     | 1     | 1     | 0     | 0     | 0     |





# Decoder: Logic Diagram





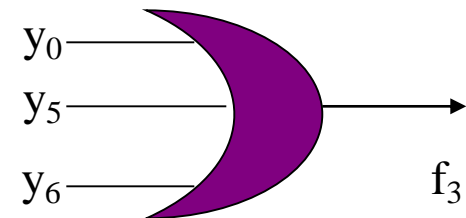
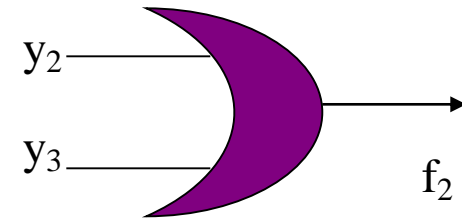
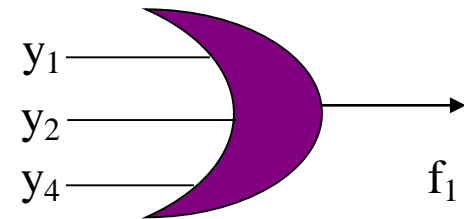
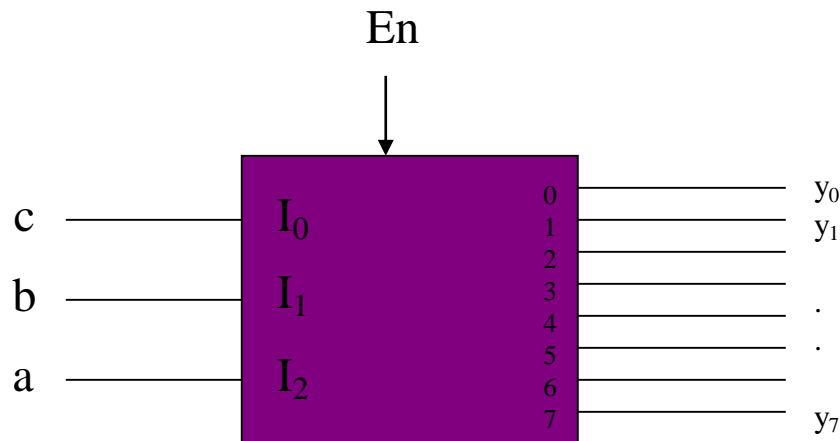
# Decoder Application: universal set {Decoder, OR }



Example: Implement functions  $f_1(a,b,c) = \sum m(1,2,4)$

$f_2(a,b,c) = \sum m(2,3)$ , and  $f_3(a,b,c) = \sum m(0,5,6)$

with a 3-input decoder and OR gates.

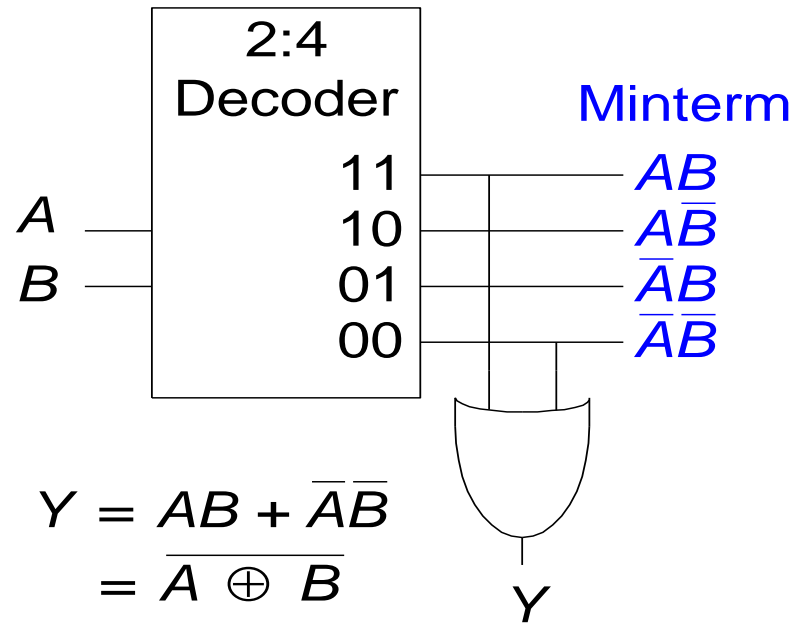




# Decoders



- OR minterms



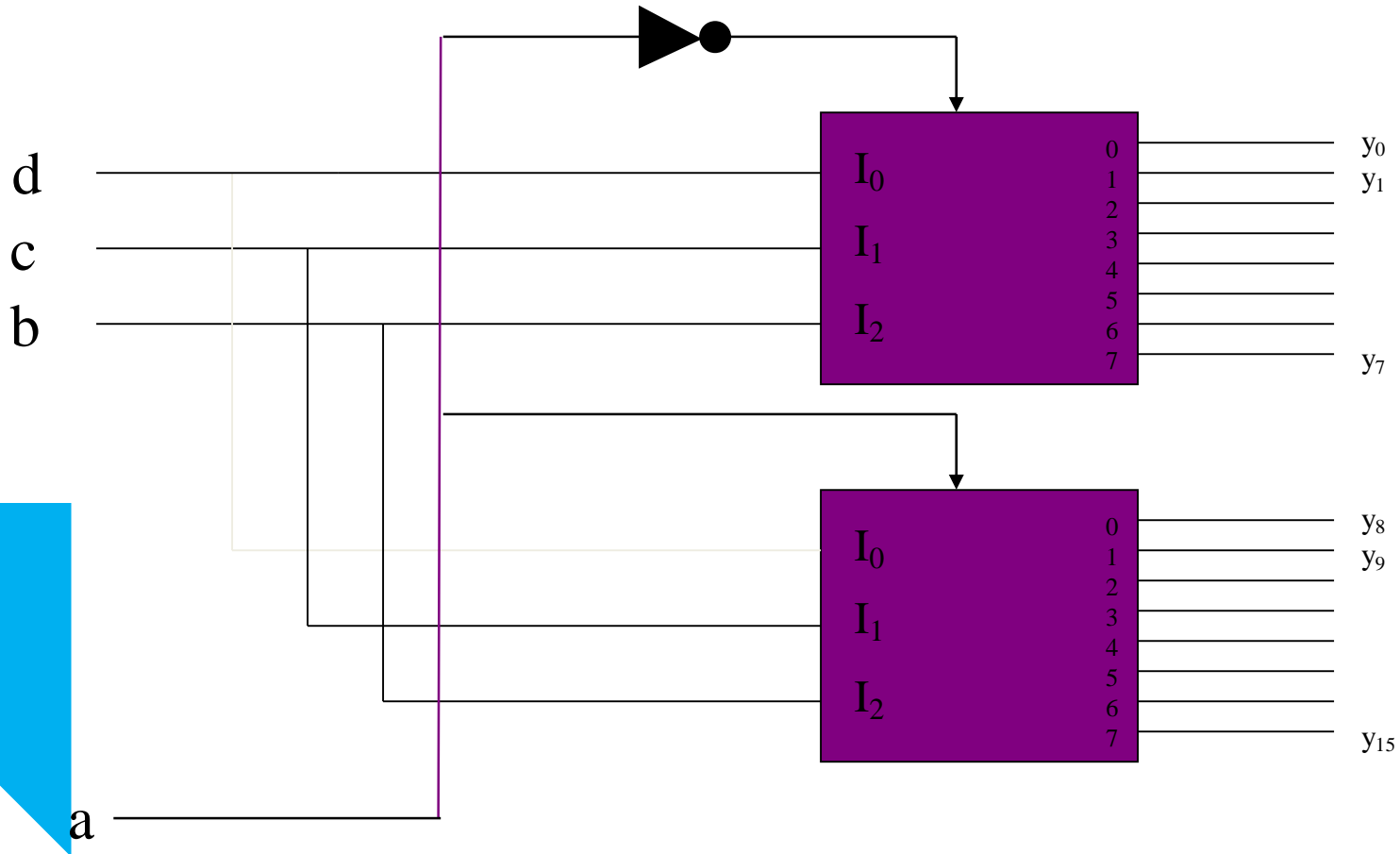




# Tree of Decoders



Implement a  $4\text{-}2^4$  decoder with  $3\text{-}2^3$  decoders.

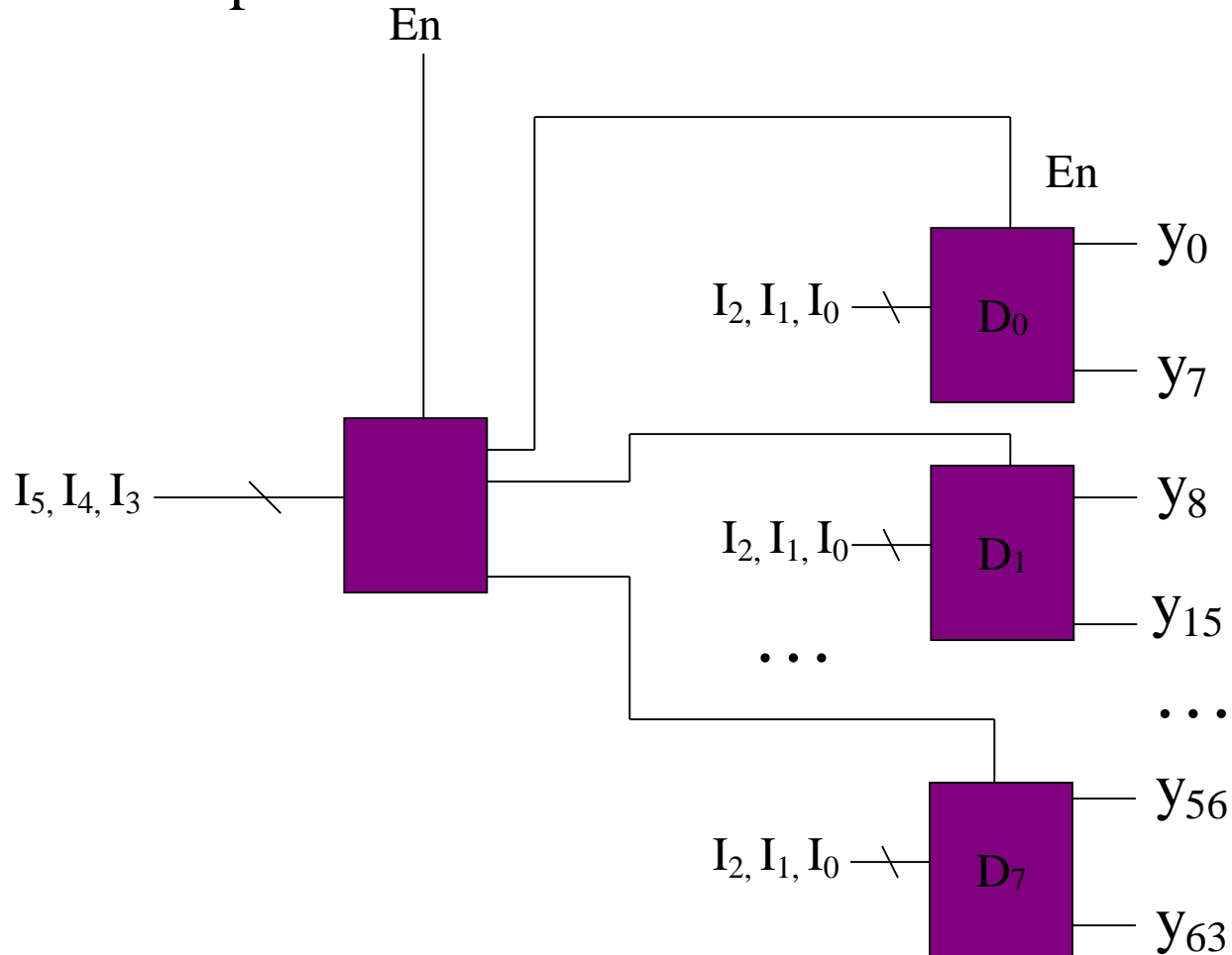




# Tree of Decoders



Implement a  $6\text{-}2^6$  decoder with  $3\text{-}2^3$  decoders.





## 2. Encoder

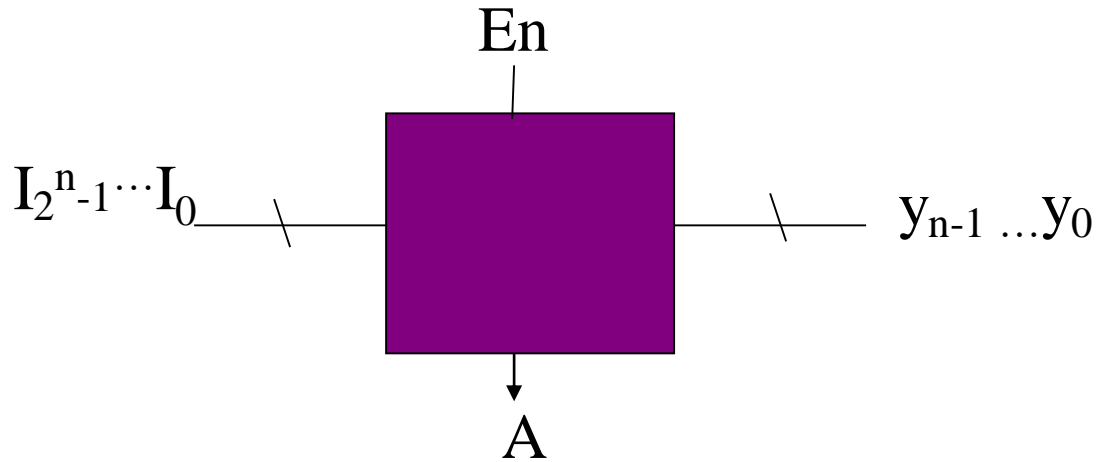


- Definition
- Logic Diagram
- Priority Encoder

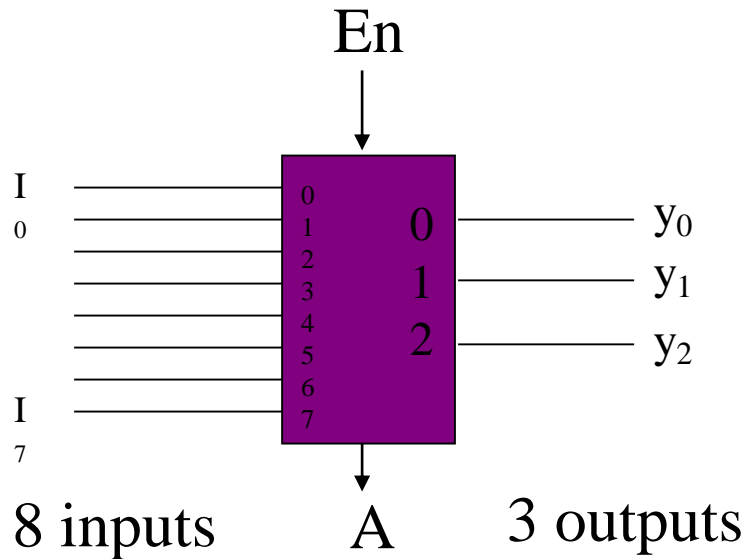




## 2. Encoder: Definition



### Encoder Description:



At most one  $I_i = 1$ .

$(y_{n-1}, \dots, y_0) = i$  if  $I_i = 1$  &  $En = 1$

$(y_{n-1}, \dots, y_0) = 0$  otherwise.

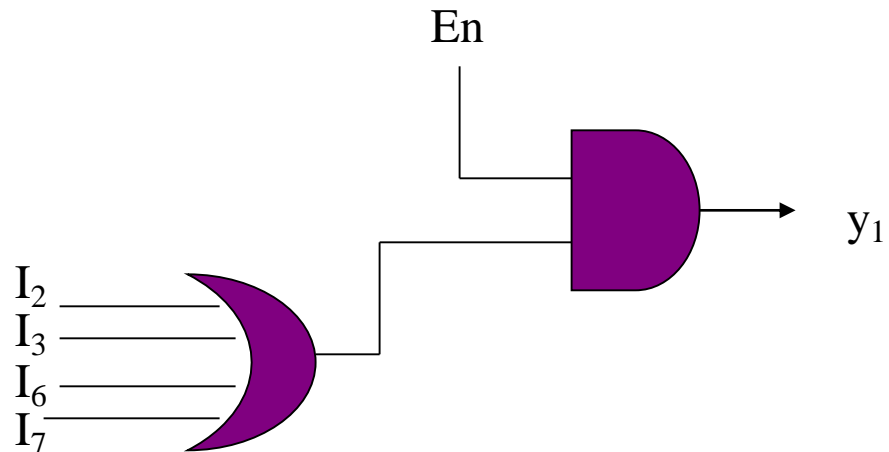
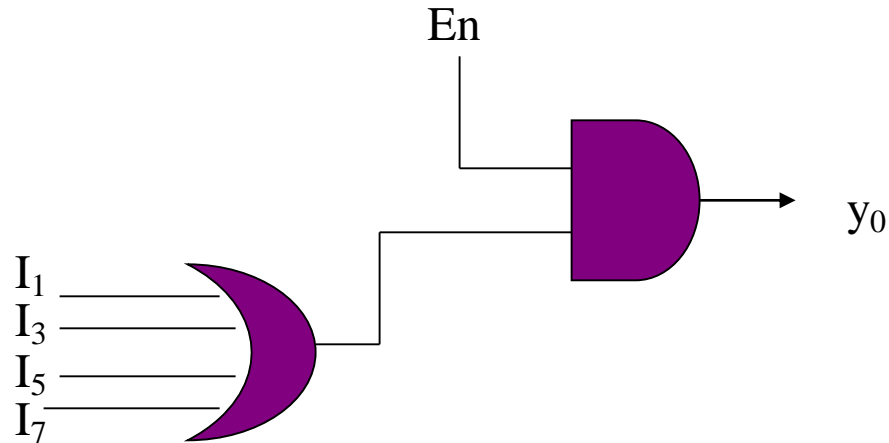
$A = 1$  if  $En = 1$  and one  $i$  s.t.  $I_i = 1$

$A = 0$  otherwise.



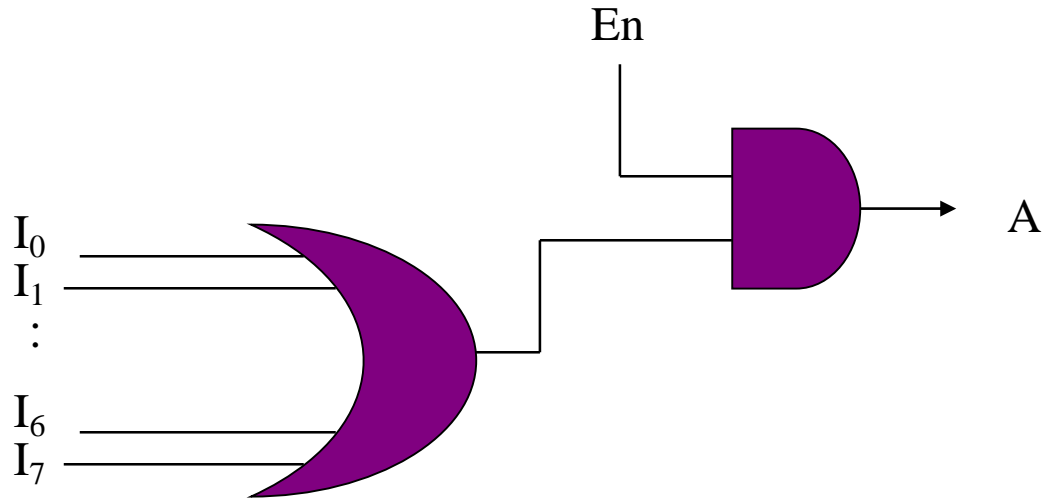
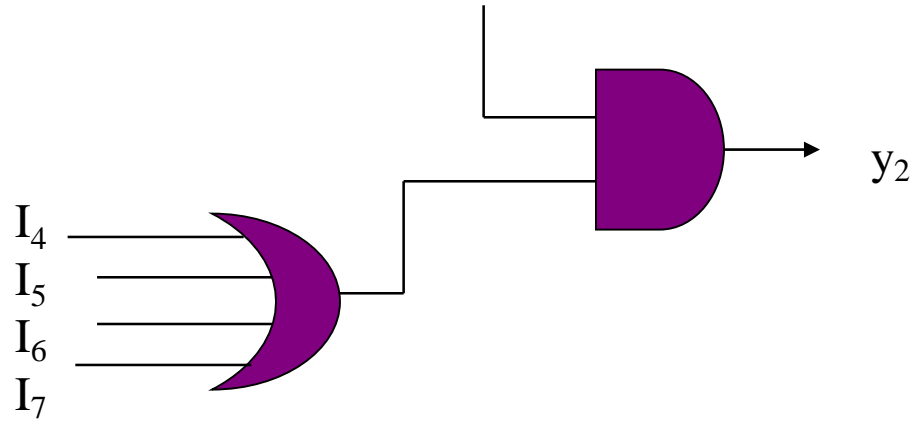


# Encoder: Logic Diagram





# Encoder: Logic Diagram





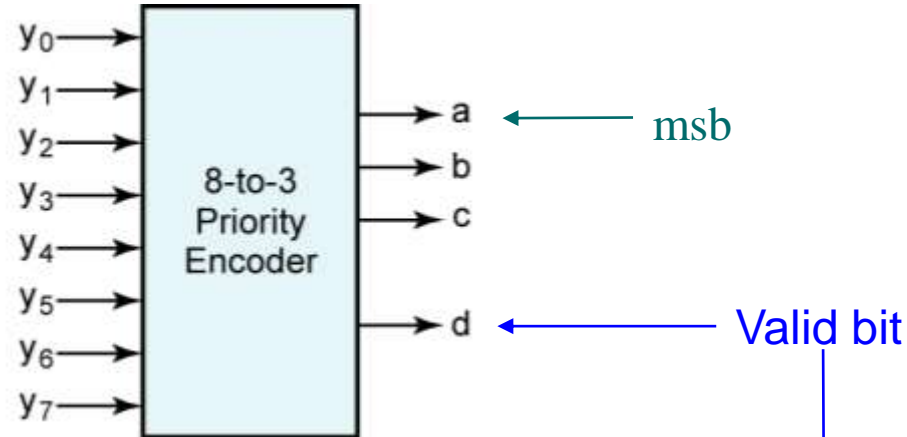
# Priority Encoders

- If more than one input is active, the higher-order input has priority over the lower-order input.
  - The higher value is encoded on the output
- A valid indicator,  $d$ , is included to indicate whether or not the output is valid.
  - Output is invalid when no inputs are active
    - $d = 0$
  - Output is valid when at least one input is active
    - $d = 1$





# Priority Encoders



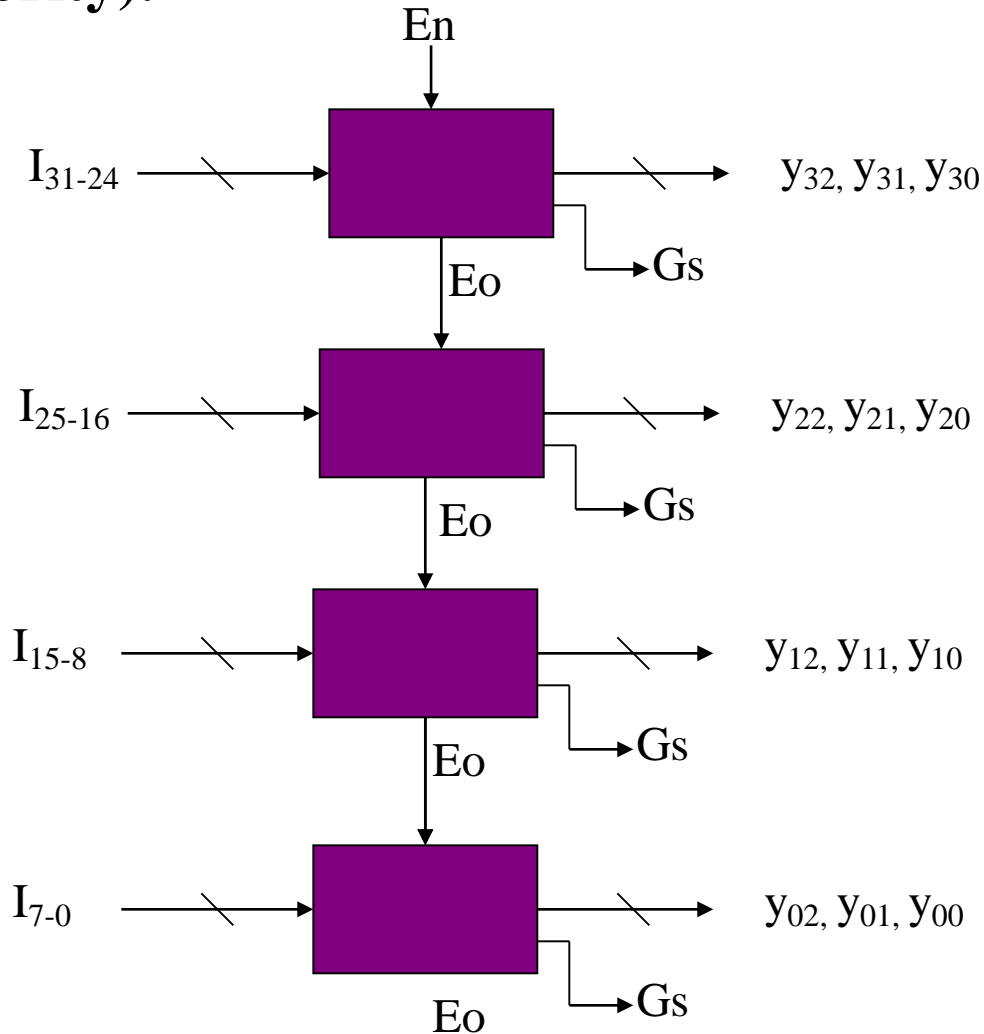
| $y_0$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ | $y_5$ | $y_6$ | $y_7$ | a | b | c | d |
|-------|-------|-------|-------|-------|-------|-------|-------|---|---|---|---|
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0 | 0 | 0 | 0 |
| 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0 | 0 | 0 | 1 |
| X     | 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0 | 0 | 1 | 1 |
| X     | X     | 1     | 0     | 0     | 0     | 0     | 0     | 0 | 1 | 0 | 1 |
| X     | X     | X     | 1     | 0     | 0     | 0     | 0     | 0 | 1 | 1 | 1 |
| X     | X     | X     | X     | 1     | 0     | 0     | 0     | 1 | 0 | 0 | 1 |
| X     | X     | X     | X     | X     | 1     | 0     | 0     | 1 | 0 | 1 | 1 |
| X     | X     | X     | X     | X     | X     | 1     | 0     | 1 | 1 | 0 | 1 |
| X     | X     | X     | X     | X     | X     | X     | 1     | 1 | 1 | 1 | 1 |







# Priority Encoder: Implement a 32-input priority encoder w/ 8 input priority encoders (high bit priority).





Thank  
you

