SNS COLLEGE OF ENGINEERING

Coimbatore-35
An Autonomous Institution

Accredited by – AICTE and Accredited by NAAC – UGC with 'A+' Grade
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19EC505–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 3 –TWIN-TUB PROCESS

OUTLINE

- INTRODUCTION
- SIX MASKS
- TWIN TUB PROCESS: N-WELL / P-WELL
- TWIN TUB PROCESS: POLYSILICON
- ACTIVITY
- TWIN TUB PROCESS: N+/ P+ DIFFUSION
- TWIN TUB PROCESS: CONTACT / VIA / METAL
- TWIN TUB PROCESS: CROSS SECTION VIEW
- ASSESSMENT
- SUMMARY

INTRODUCTION

n-well: The pMOS transistors are placed in the n-well and the nMOS transistors are created on the substrate

p-well: The nMOS transistors are placed in the p-well and the pMOS transistors are created on the substrate

n-well + p-well =Twin tub Process

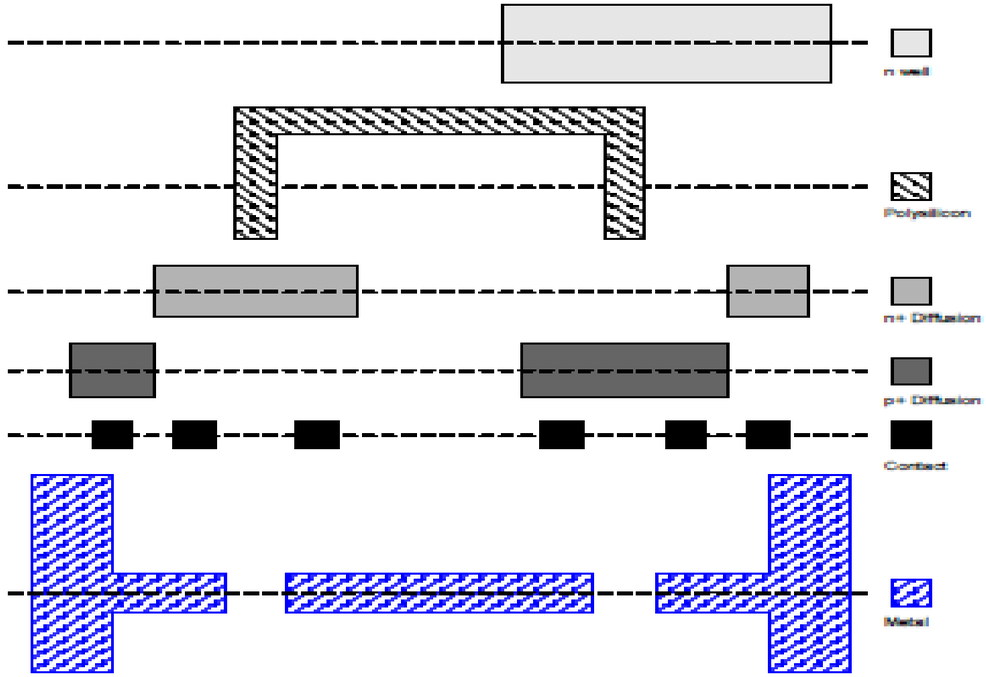
SIX MASKS

•Twin-tub CMOS technology provides the basis for ***separate optimization*** of the **p-type and n-type transistors**.

•One can optimize independently for ***threshold voltage***, ***body effect***, and the ***gain*** associated with n- and p-devices

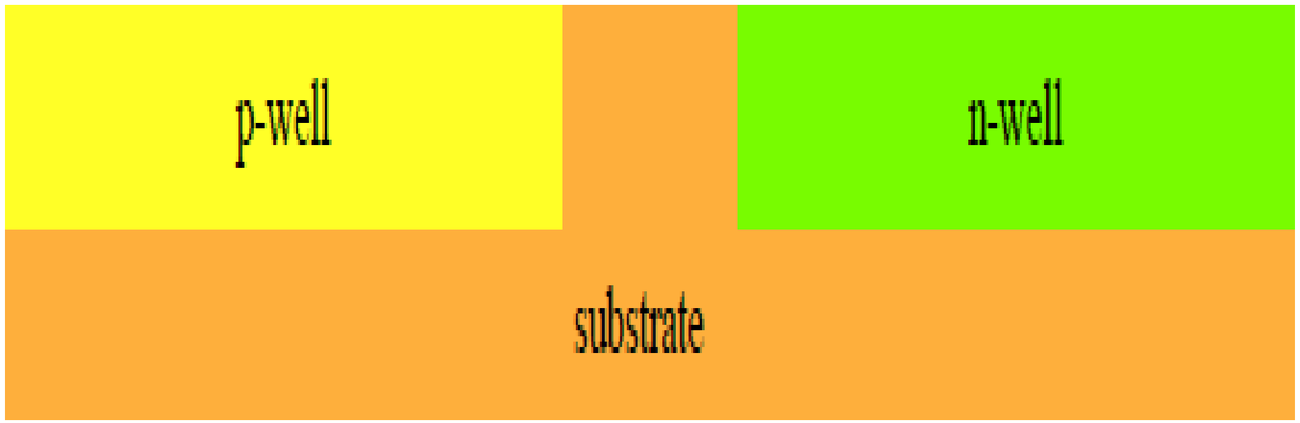
Six masks

– n/p-well
– Polysilicon
– n+ /p+ diffusion
– p+/n+ diffusion
– Contact
– Metal



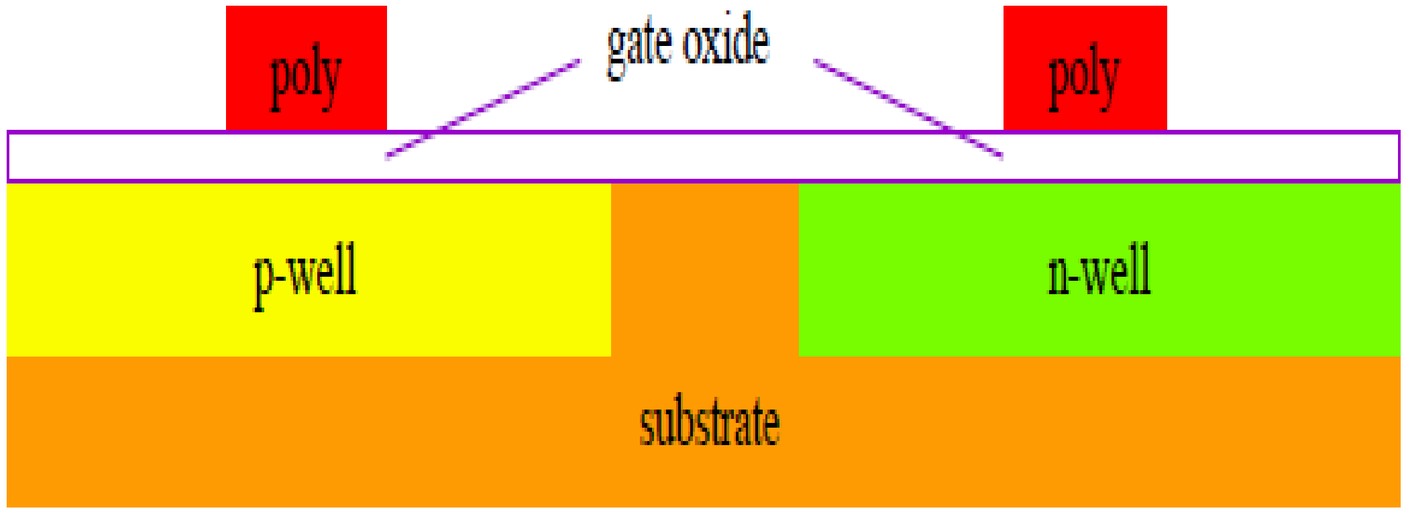
TWIN TUB PROCESS: N-WELL / P-WELL

First place wells to provide properly-doped substrate for n-type, p-type transistors:



TWIN TUB PROCESS: POLYSILICON

Pattern polysilicon before diffusion regions:

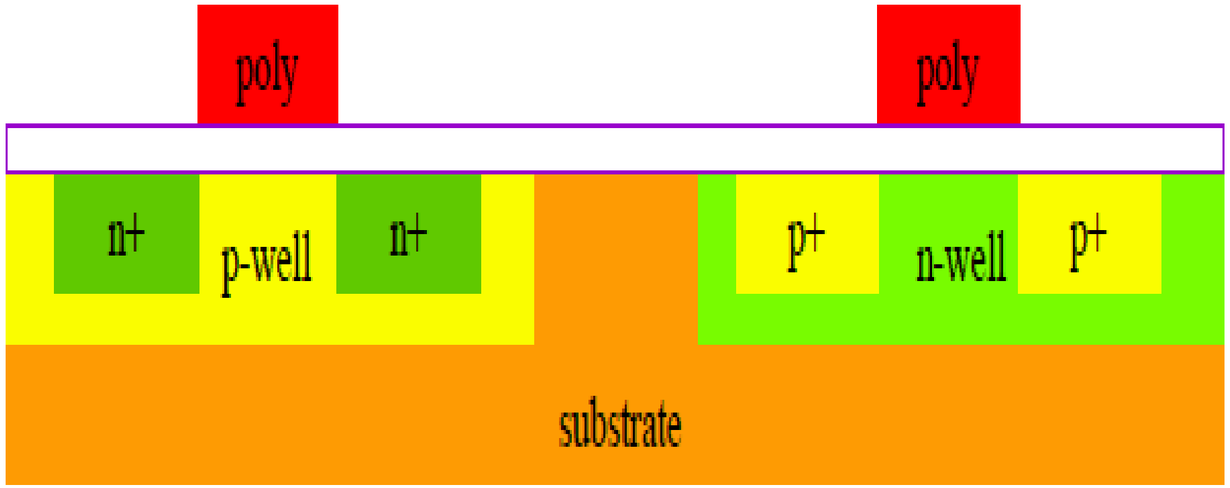


ACTIVITY-BRAIN TEASERS

51	11	61
64	30	32
35	?	43

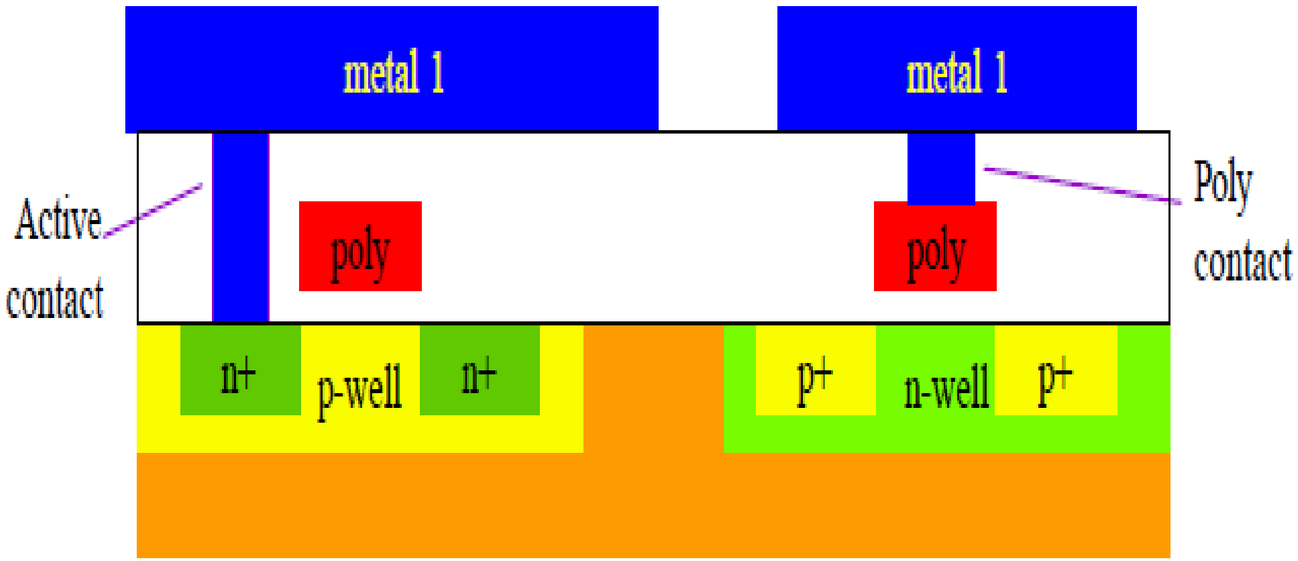
TWIN TUB PROCESS: N+/ P+ DIFFUSION

Add diffusions, performing self-masking:

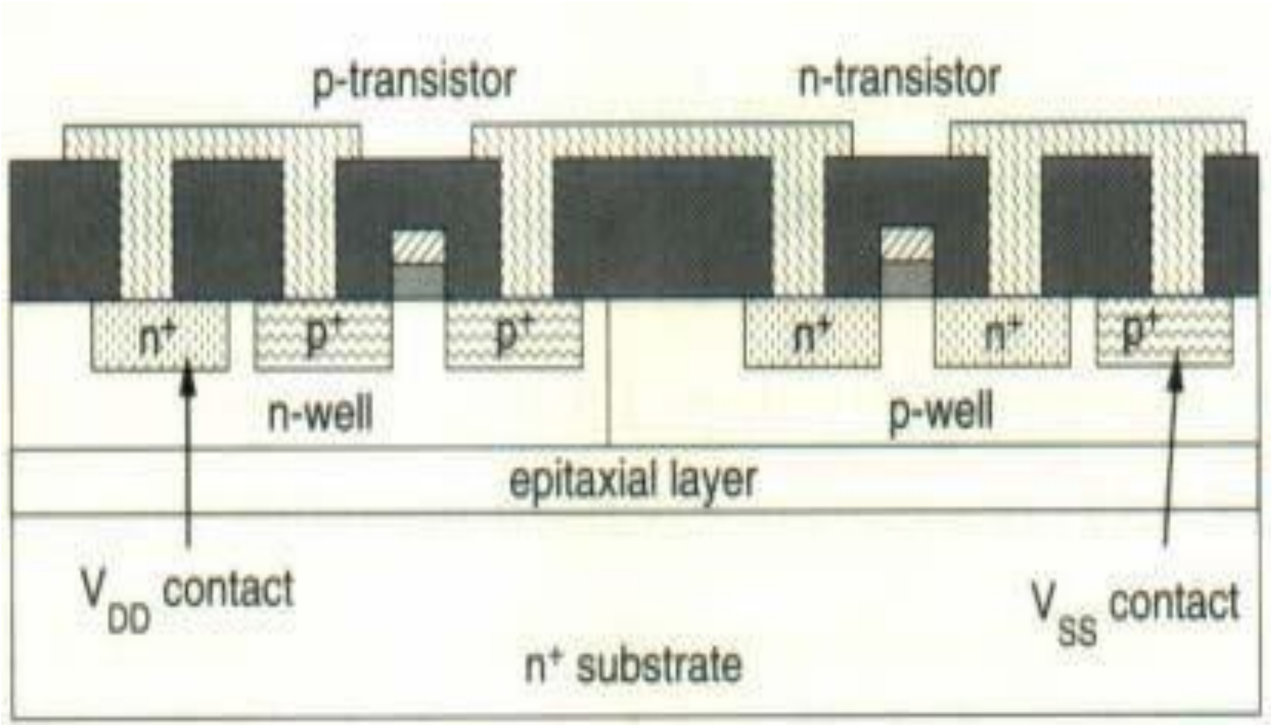


TWIN TUB PROCESS: CONTACT / VIA / METAL

Start adding metal layers:



CROSS SECTIONAL VIEW OF TWIN TUB PROCESS



ASSESSMENT

1.List out the steps involved in Twin tub process

2.List out the six masking levels.

3.Draw the Cross sectional view of Twin tub process

THANK YOU