SNS COLLEGE OF ENGINEERING

Coimbatore-35
An Autonomous Institution

Accredited by – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

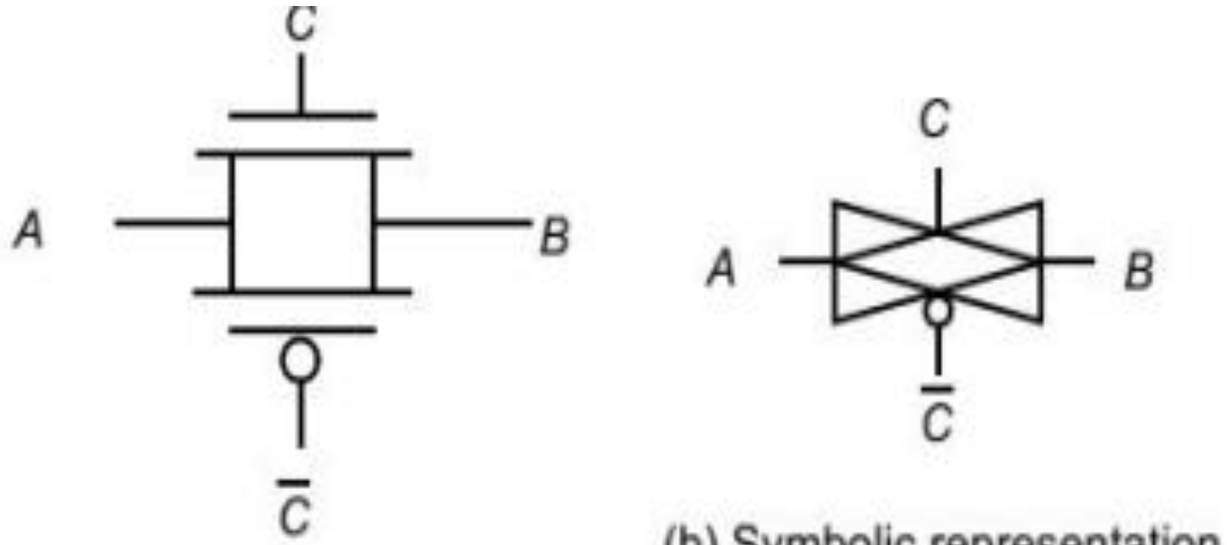
19EC505–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS
TOPIC –Transmission Gate Logic

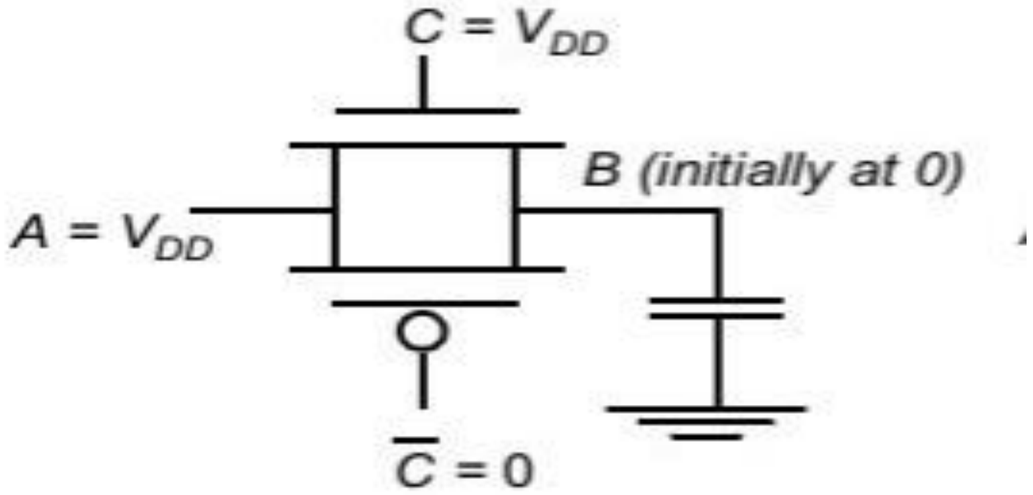
Transmission Gate Logic

- The most widely-used solution to deal with the voltage-drop problem is the use of transmission gates.
- It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0.
- The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up.
- The transmission gate combines the best of both device flavors by placing a NMOS device in parallel with a PMOS device. The control signals to the transmission gate (C and C) are complementary



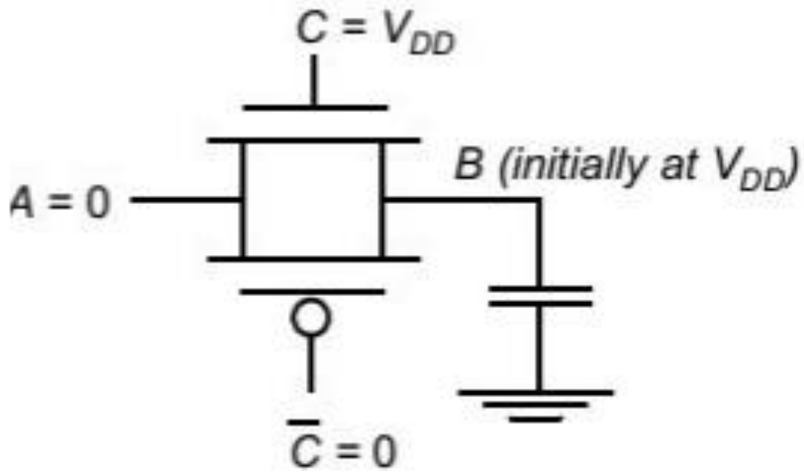
CMOS transmission gate

Transmission gates enable rail-to-rail switching



(a) charging node B

Transmission gates enable rail-to-rail switching



(a) discharging node B

THANK YOU