SNS COLLEGE OF ENGINEERING

Computer organisation and Architecture

UNIT-III

1. Define MIPS .
2. Define MIPS Rate:
3. Define pipelining.
4. Define parallel processing.
5. Define instruction pipeline.
6. What are the steps required for a pipelinened processor to process the instruction?
7. What are Hazards?
8. State different types of hazards that can occur in pipeline.
9. Define Data hazards
10. Define Instruction hazards
11.Define Structural hazards?
12. What are the classification of data hazards?
13.Define RAW hazard : (read after write)
14. Define WAW hazard :(write after write)
15.Define WAR hazard :(write after read)
16. How data hazard can be prevented in pipelining?
17.How Compiler is used in Pipelining?
18. How addressing modes affect the instruction pipelining?
19. What is locality of reference?
20. What is the need for reduced instruction chip?
21. Define memory access time?
22. Define memory cycle time.
23.Define Static Memories.
24. List out Various branching technique used in micro program control unit?
25. How the interrupt is handled during exception?
26. List out the methods used to improve system performance.
27. What are the ways to build a datapath
28. What are the control schemes available in processors

PART B

1. State and explain the different types of hazards that can occur in a pipeline.
2.Draw and explain the structure of a superscalar processor. Also explain the flow of instruction
execution in it.
3. Explain the control implementation scheme in detail
4. Implement basic structure of MIPS
5. Define data hazard and instruction hazard and explain in detail
6. Explain pipelined data path and control path
7. What are the two aspects of machine instruction? Explain it .

8. .Draw and explain the modified three-bus structure of the processor suitable for four -stage
pipelined execution. How this structure is suitable to provide four-stage pipelined execution?