SNS COLLEGE OF ENGINEERING

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19EC505–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC –POWER DISSIPATION

OUTLINE

- INTRODUCTION
- MOTIVATION TO ESTIMATE POWER DISSIPATION
- SOURCES OF POWER DISSIPATION
- DYNAMIC POWER DISSIPATION
- ACTIVITY
- STATIC POWER DISSIPATION
- METRICS
- ASSESSMENT
- SUMMARY

INTRODUCTION -WHY WORRY ABOUT POWER?

- ➢Battery-powered devices
  - •GSM phone, UMTS phone, MP3 player, PDAs
    - •Complexity increases
    - •Energy budget remains the same
- ➢Complex high-speed devices
  - •Thermal problems
  - •Expensive packaging

Power dissipation affects

- •Performance
- •Reliability
- •Packaging
- •Cost
- •Portability

OVERVIEW OF POWER CONSUMPTION

- **The total power dissipation in CMOS Circuit can be expressed in three main components.**

1. Static power dissipation (due to leakage current when the circuit is idle).
2. Dynamic power dissipation (When the circuit is switching).
3. Short – Circuit power dissipation during switching of transistors.

OVERVIEW OF POWER CONSUMPTION

- $P_{\text{total}} = \mathbf{P}_{\textbf{dynamic}} + \mathbf{P}_{\textbf{short-circuit}} + \mathbf{P}_{\textbf{leakage}} + \mathbf{P}_{\textbf{static}}$

➢ Dynamic (Switching) Power Consumption ($\mathbf{P}_{\textbf{dynamic}}$)
  - Charging and discharging capacitors

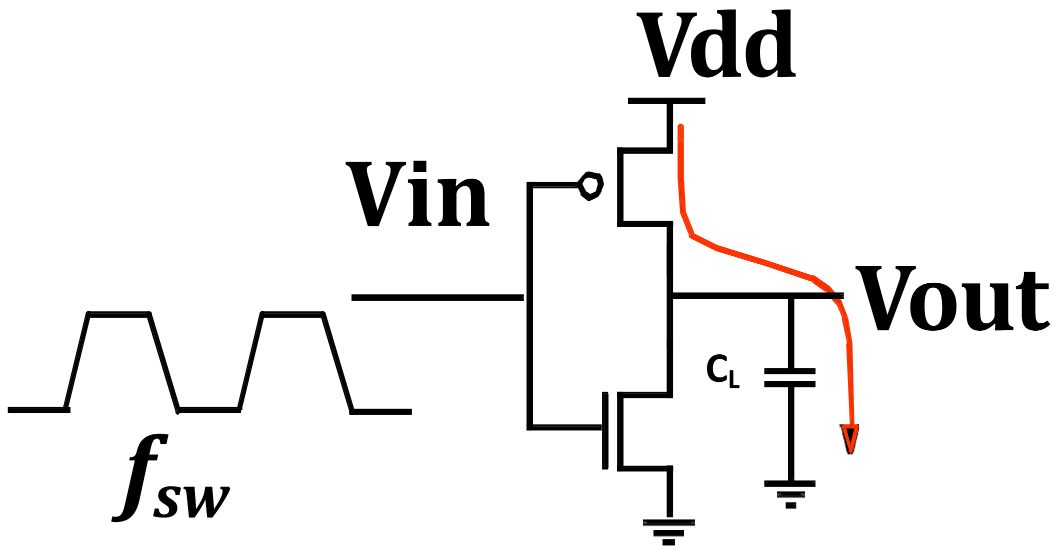
➢ Short Circuit Power Consumption ($\mathbf{P}_{\textbf{short-circuit}}$)
  - Short circuit path between supply rails during switching

➢ Leakage Power Consumption ($\mathbf{P}_{\textbf{leakage}}$)
  - Leaking diodes and transistors

➢ Static Power Consumption ($\mathbf{P}_{\textbf{static}}$)

DYNAMIC POWER

- Dynamic power dissipation occurs when the MOS transistor switches to charge and discharge load capacitances.
- Consumes most of the power in CMOS Circuits.
- One cycle involves a rising and falling output.
- On rising output, charge $\boldsymbol{Q = CV_{DD}}$ is required
- On falling output, charge is dumped to GND



DYNAMIC POWER

- **Energy Per Transition**
  - Not a function of frequency!
  - 50% dissipated by Ron
  - 50% stored/delivered in/by CL
- **Dynamic Power**

$$P_{dynamic} = C_L \times V_{DD}^2 \times f$$

C_L - Total output node capacitance.

V_{DD}^2 - Supply voltage at which the output capacitance charges

f- Operating frequency.

- Not a function of transistor sizes!
- Need to reduce C_L, V_{DD}, and f to reduce power.

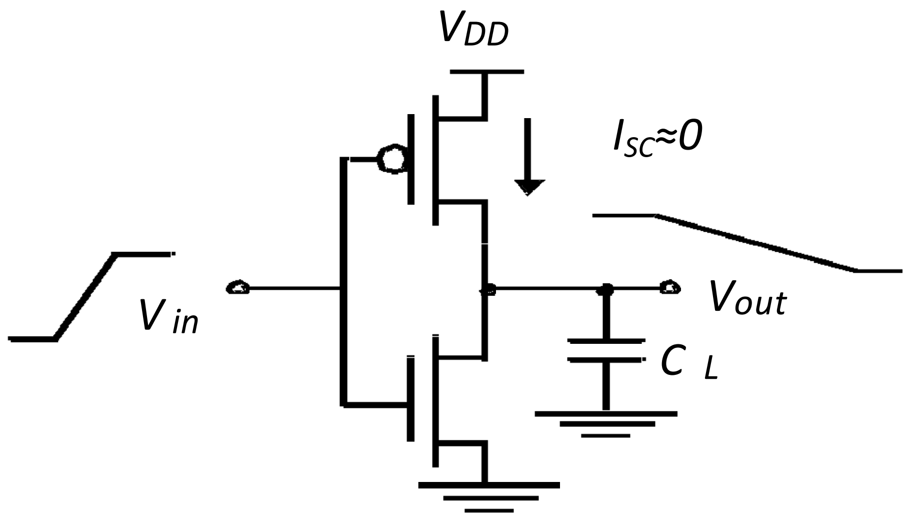
SHORT CIRCUIT CURRENT (1/2)

- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of "short circuit" current.
- ~ 15% of dynamic power
  - ~85% to charge capacitance $\mathbf{C_L}$
- NMOS and PMOS on
  - Both transistors in saturation
- Long rise / fall times
  - Slow input transition
  - Increase short circuit current

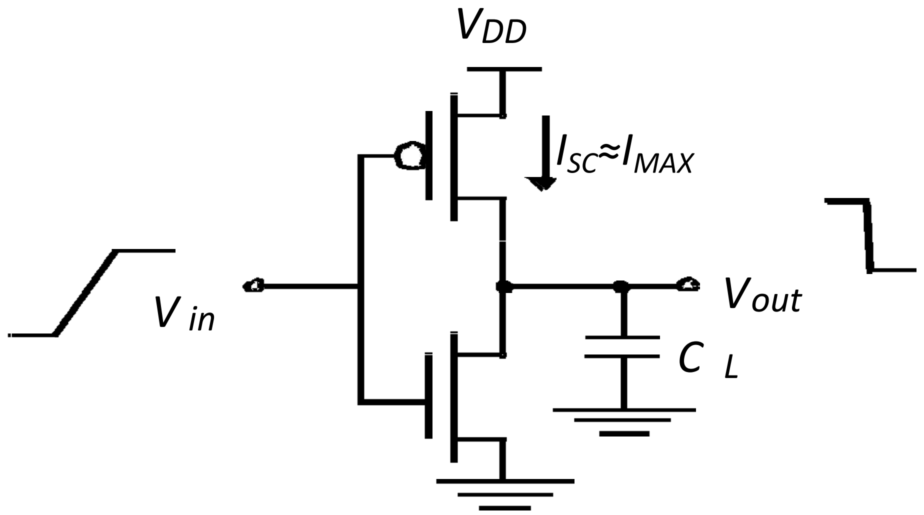
Make input signal transitions fast to save power!

SHORT CIRCUIT CURRENT (2/2)

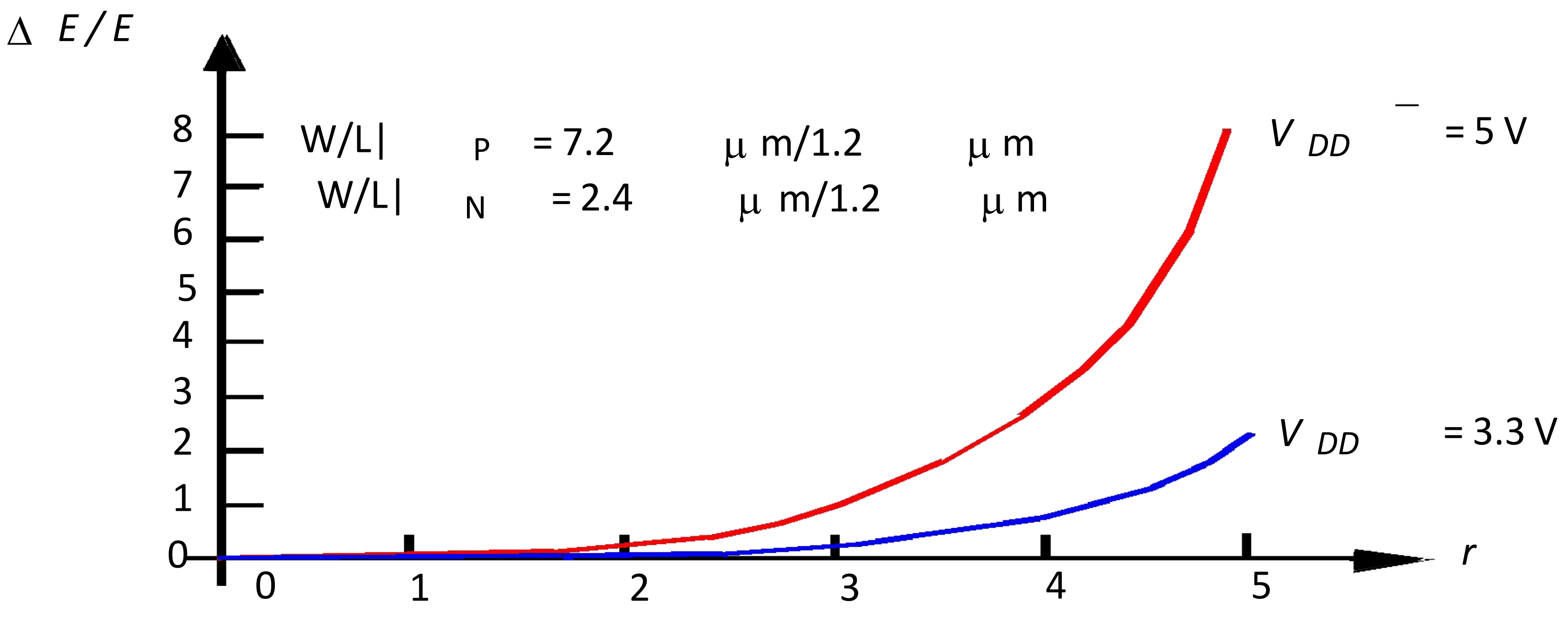
Because of finite slope of input signal, there is a period when both PMOS and NMOS device are “on” and create a path from supply to ground



Large capacitive load



Small capacitive load



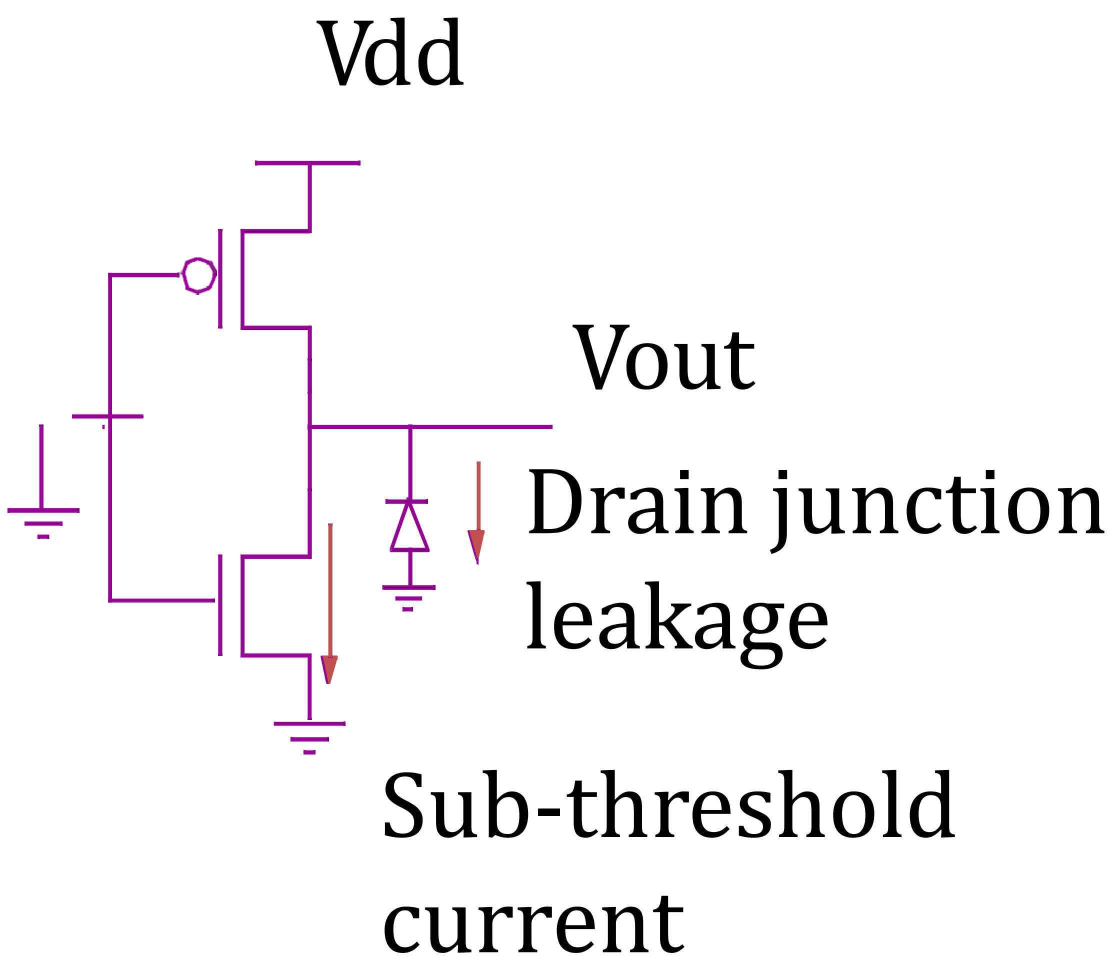
The power dissipation due to short circuit currents is minimized by matching the rise/fall times of the input and output signals.

LEAKAGE

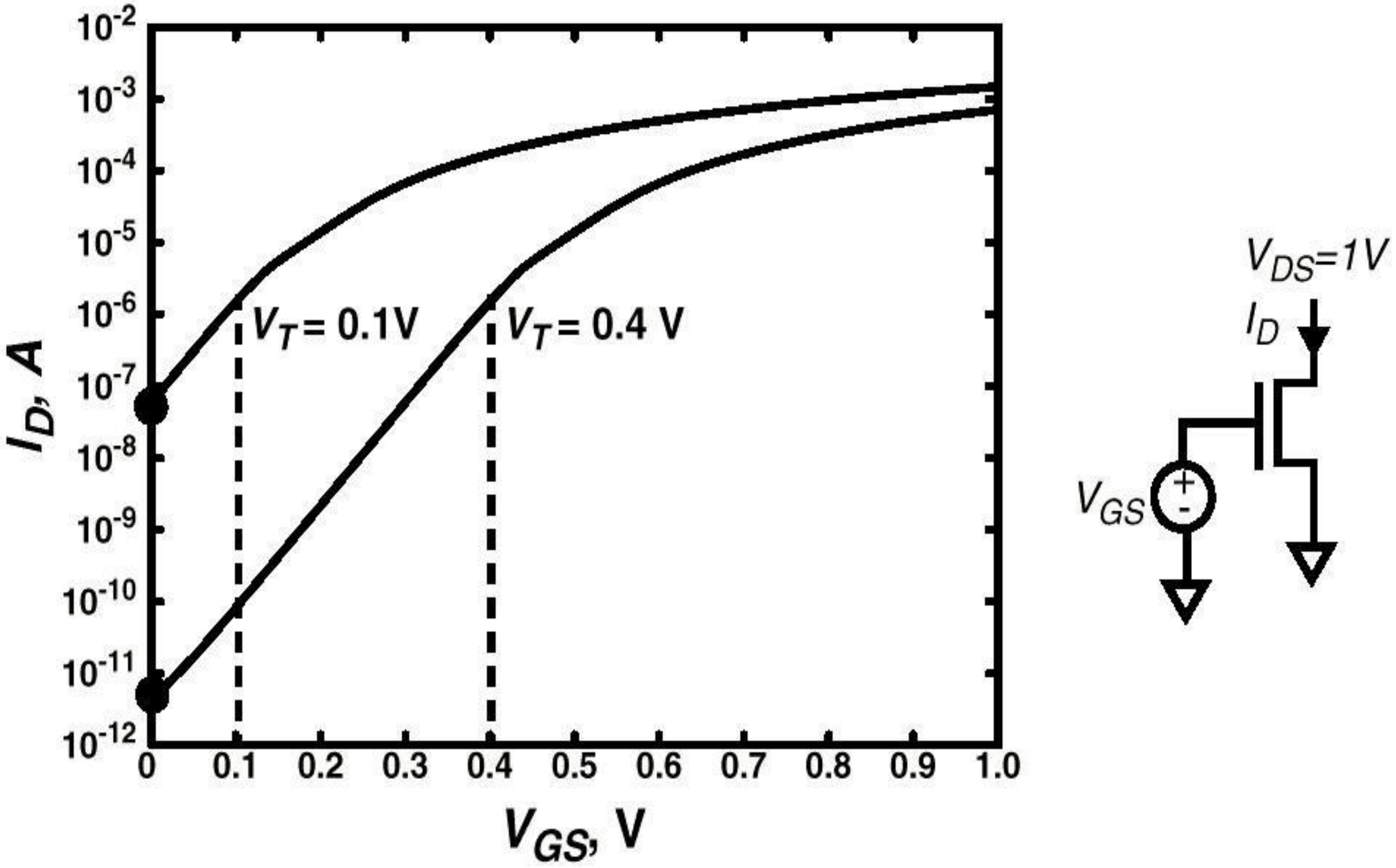
- Sub-threshold current
  - –Transistor conducts below Vt
  - –For sub-micron relevant
    - VDD / Vt ratio smaller
    - Can dominate power consumption!
    - Especially in idle mode.

  Charge nodes fully to VDD!

  Discharge nodes completely to GND!
- Drain leakage current
  - –Reverse biased junction diodes

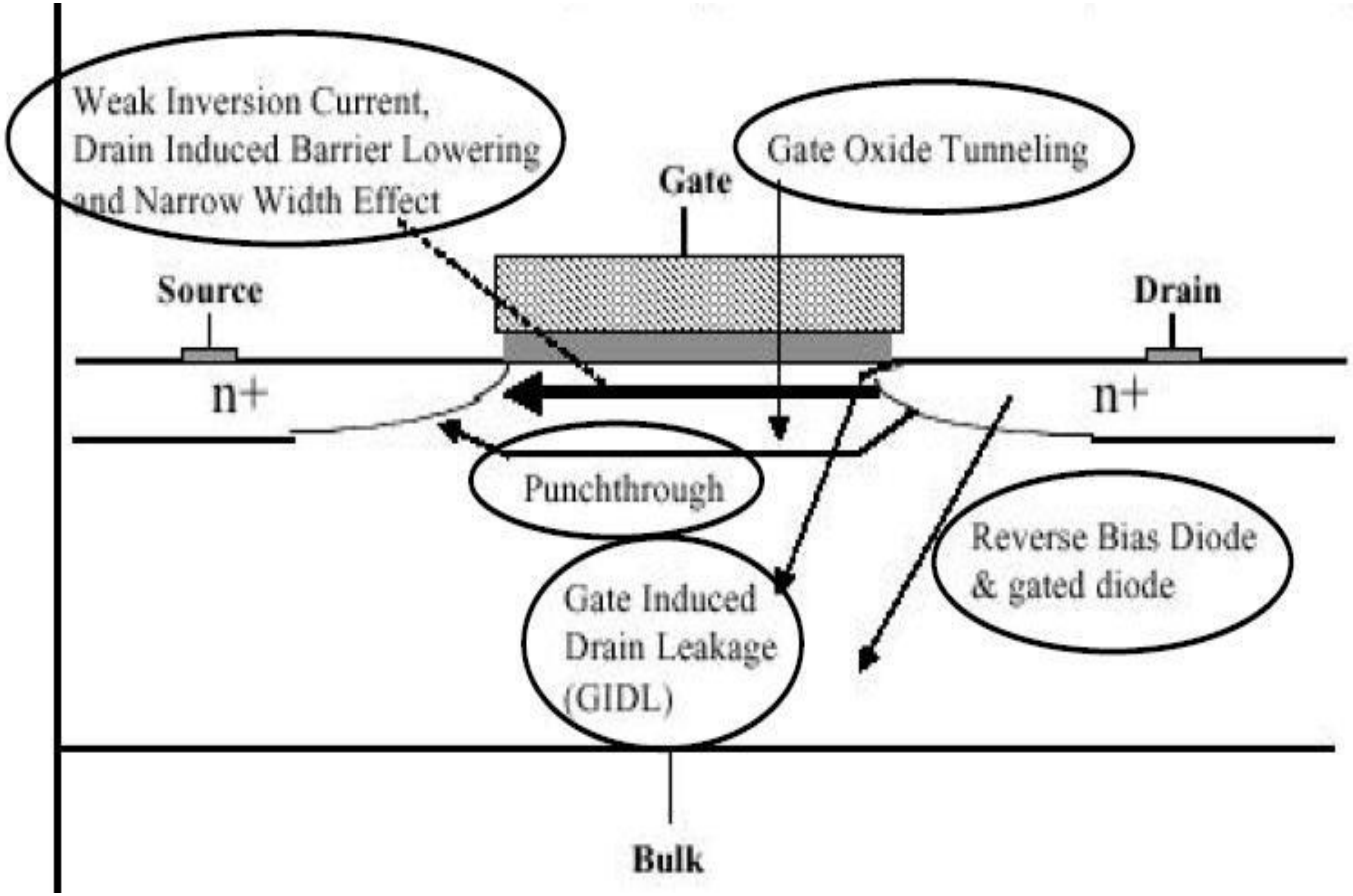


SUB-THRESHOLD LEAKAGE COMPONENT



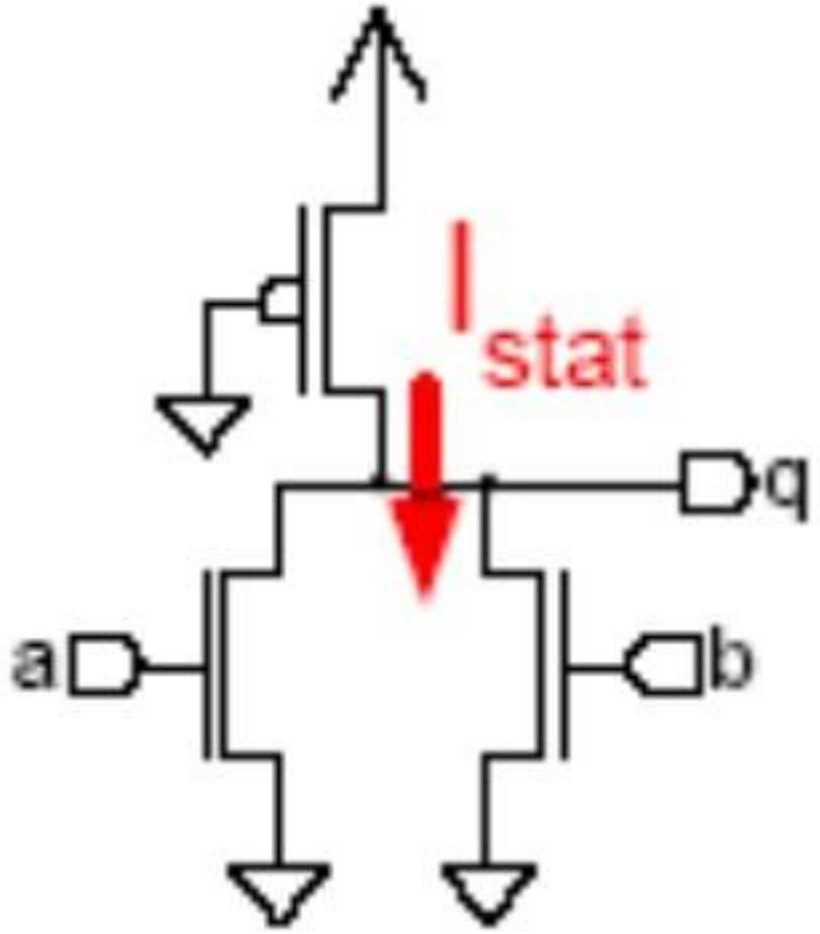
- **Leakage control is critical for low-voltage operation**

SOURCE OF LEAKAGE CURRENT



STATIC POWER CONSUMPTION

- Pseudo-NMOS logic style
  - –PMOS as resistor
  - –PDN as static CMOS logic
- Static current
  - –When output low
- Power consumption
  - –Even without switching activity



POWER DISSIPATION FOR VARIOUS CMOS CIRCUITS

Chip	Intel 386	DEC Alpha 21064	Cell based ASIC
Minimum feature size	1.5μm	0.75μm	0.5μm
Number of gates	36,808	263,666	10,000
f_{CLK}	16MHz	200MHz	110MHz
V_{DD}	5V	3.3V	3V
P_{total}	1.41W	32w	0.8w
Logic gates	32%	14%	9%
Clock Distribution	9%	32%	30%
Interconnect	28%	14%	15%
I/O drivers	26%	37%	43%

DESIGN FOR LOW POWER

- **Good Ideas**
  - –On all levels
    - Software
    - Algorithm
    - Architecture
    - Gate
    - Transistor
    - Process technology

- **Bad Ideas**
  - Apply one method
  - Do it as late as possible

DESIGN FOR LOW POWER

- **System Level**
  - –Power management
    - Power-down mode
    - Global clock gating
    - Dynamic voltage scaling
  - –Hardware/software co-design
    - Early (simplified) power estimation
    - Partitioning of functionality
    - Minimum instructions for execution not code size

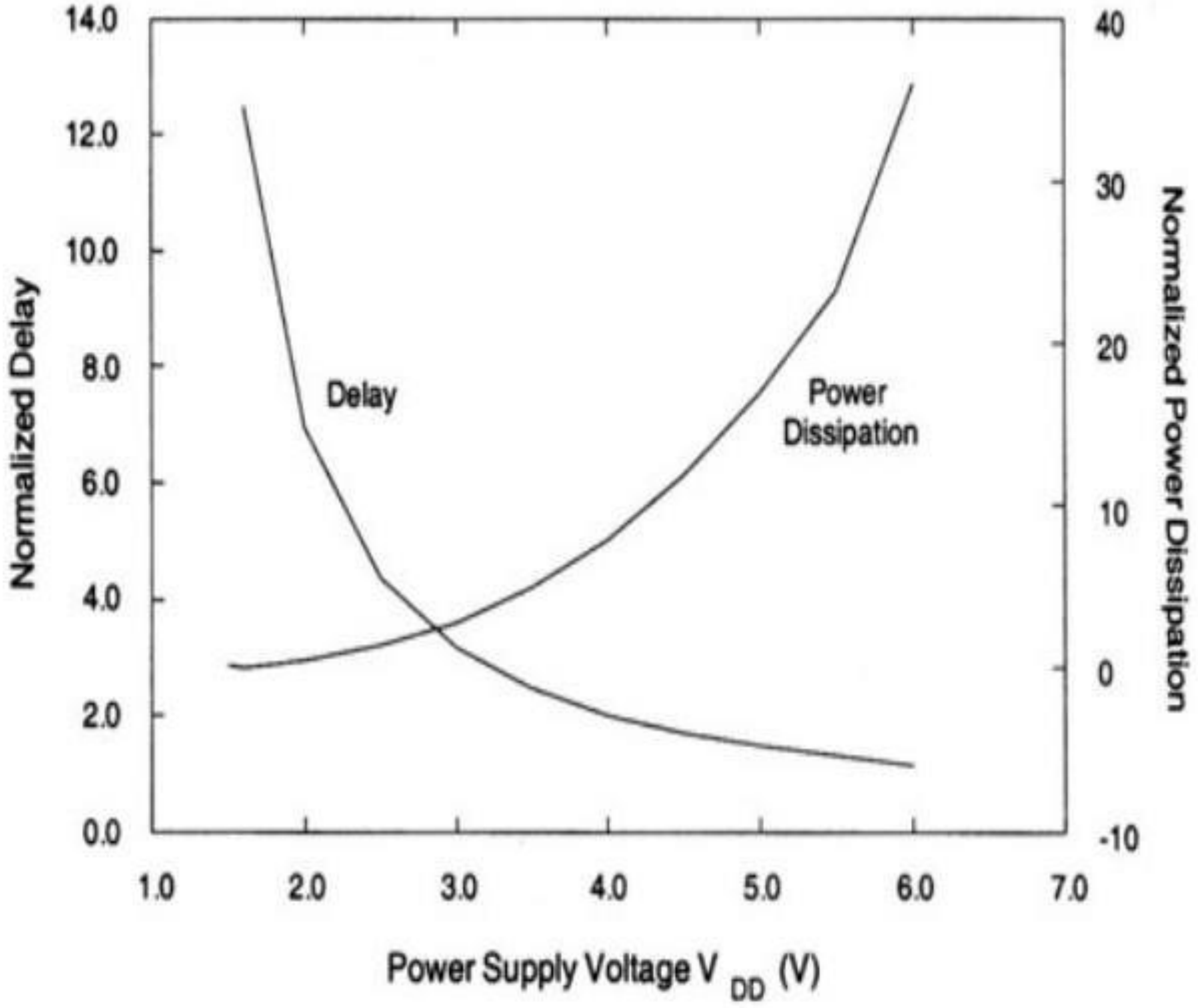
DESIGN FOR LOW POWER

- **Algorithm**
  - Arithmetic
    - Choice of number representation
    - Pre-computation
  - Concurrency
    - Parallelism - Trade area for power
    - To reduce frequency

- **Architecture**
  - Pipelining
    - Allows voltage scaling: Increased throughput because frequency could be increased => lower supply voltage instead
  - Redundancy
    - Minimize shared resources to lower signal activity (buses)
  - Data encoding
    - Energy efficient state encoding
    - Example: Gray code, One hot encoding
  - Clocking
    - Gated clocks, Self-timed circuits

VOLTAGE SCALING

- $P_{dynamic} = f \times C \times V_{DD}^2$
  - –Quadratic influence
- Delay
  - –Increased
- Power delay product
  - –Improved

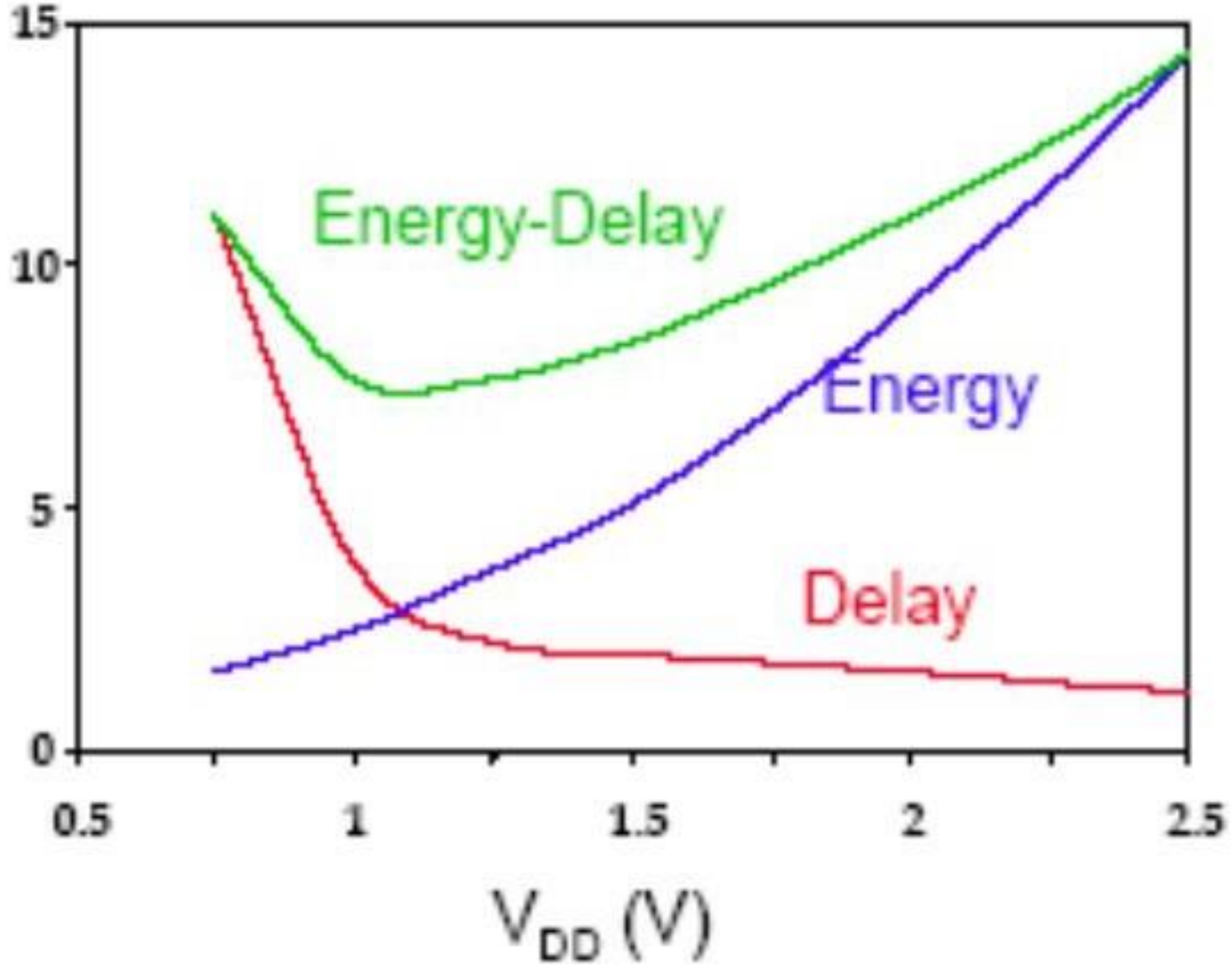


VOLTAGE SCALING

EDP (Energy Delay Product)

- –Measure for energy efficiency

- Lower supply voltage
  - –Less energy
  - –Increased delay

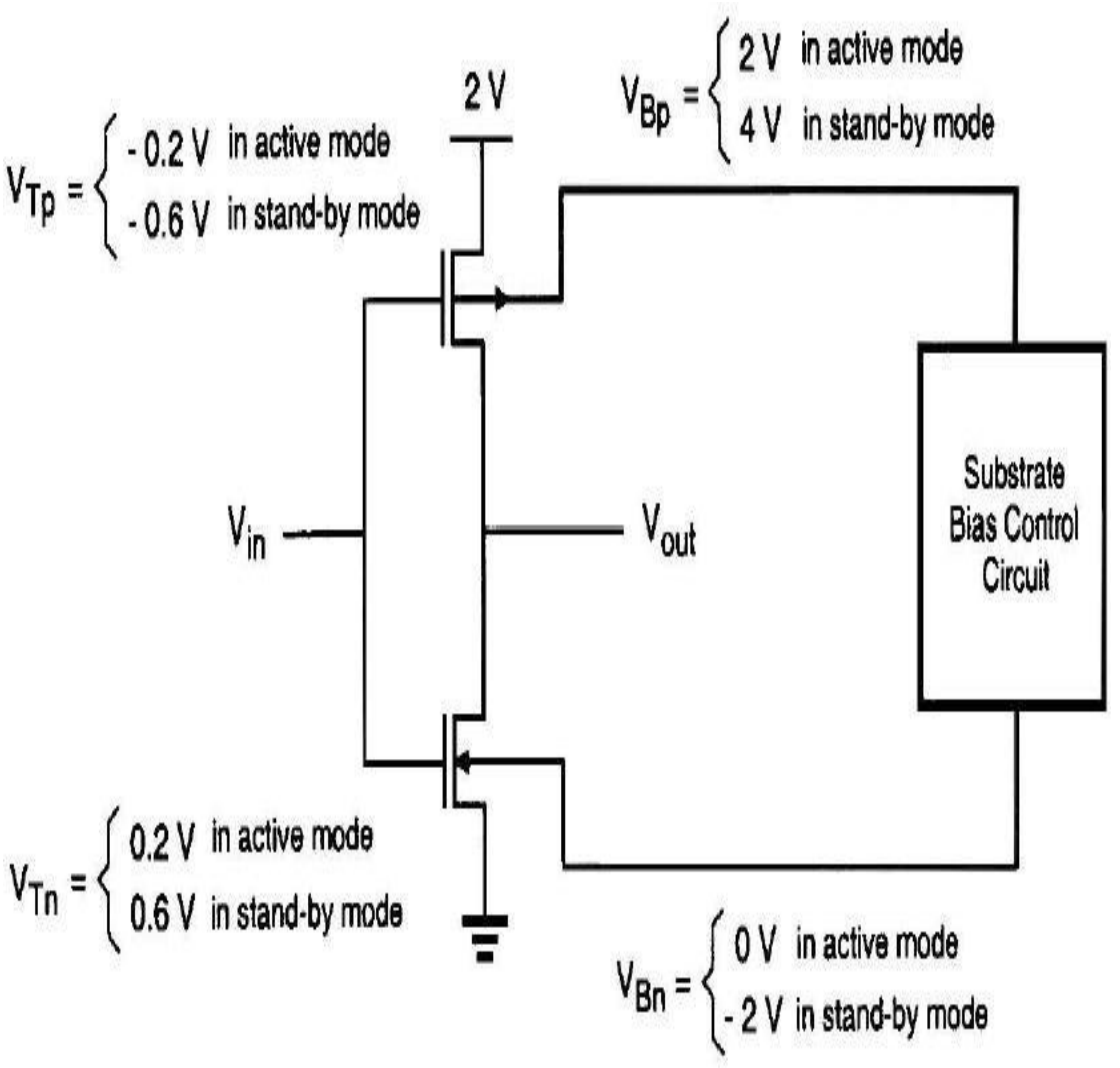


VOLTAGE SCALING

- Dual voltage supply
- Internal voltage
  - –Reduced internal voltage 1.2V
    - For low power operation
- External voltage
  - –Compatible IO voltage 3.3V
    - To interface other ICs

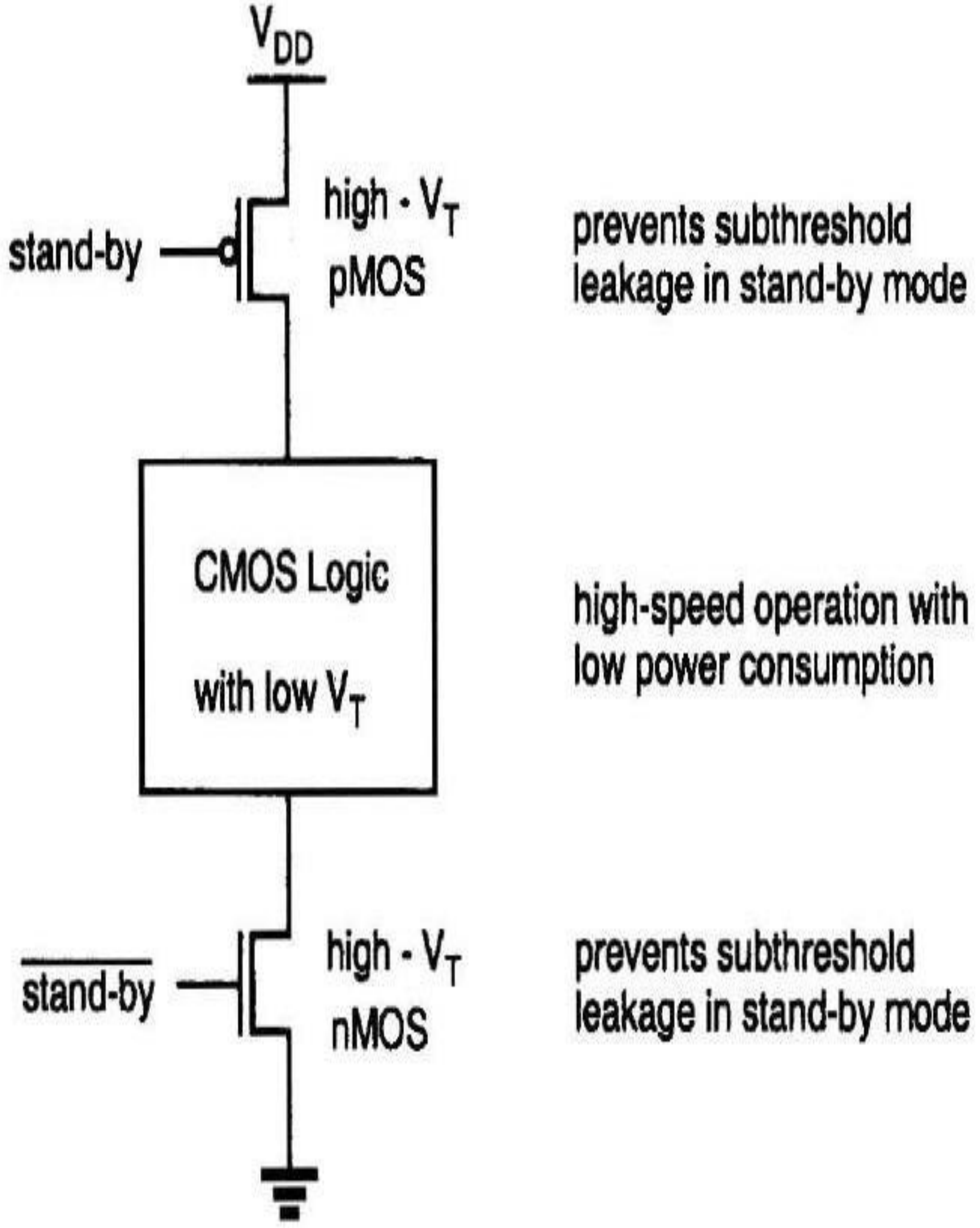
VARIABLE-THRESHOLD CMOS (VTCMOS) CIRCUITS

- An efficient way to reduce **sub threshold leakage currents**
  - –Require twin-well or triple-well CMOS technology to apply different substrate bias voltages.
  - –Separate power pins may be required if the substrate bias voltages level are not generated on-chip.



MULTIPLE-THRESHOLD CMOS (MTCMOS) CIRCUITS

- **Active Mode**
  - –High-V_T transistors are turned on.
  - –Logic gates consisting of low-V_T transistors can operate with low switching power dissipation and small propagation delay.
- **Standby Mode**
  - –High-V_T transistors are turned off, and the conduction paths can be effectively cut off.
- The series-connected standby transistors increase the overall circuit area and add extra parasitic capacitance and delay.



SWITCHING ACTIVITY REDUCTION (1/5)

Power Consumption is Data Dependent

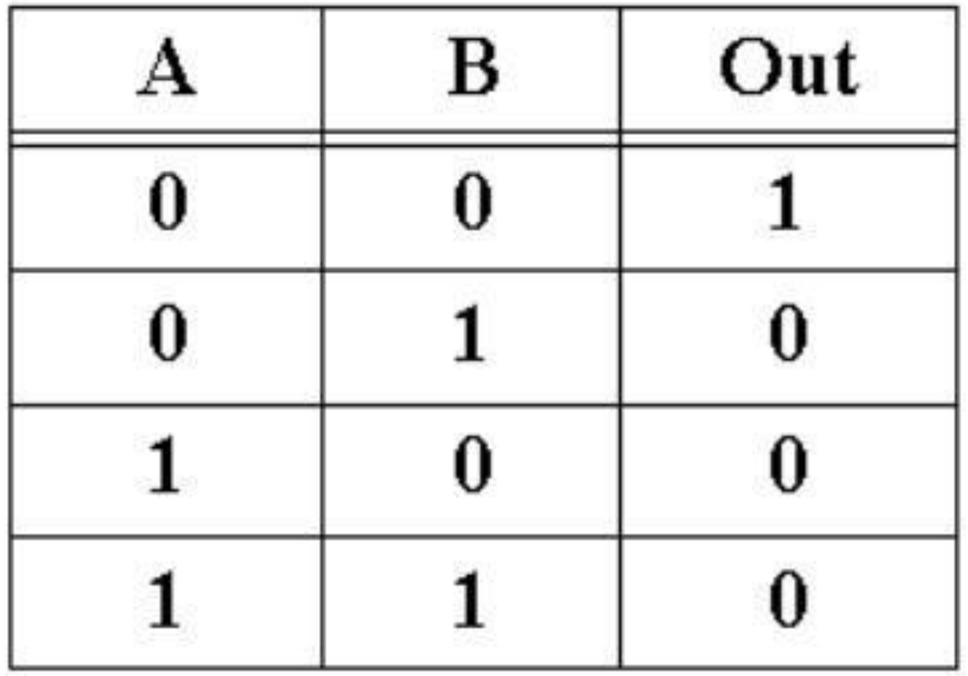
- Static Circuit
  - Example 1: 2 input static NOR gate

    Assume $P(A=1)=1/2$, $P(B=1)=1/2$.

    $P(out=1)=1/4$

    $P_{0\rightarrow 1}=P(out=0)P(out=1)=3/4\times 1/4=3/16$

    $C_{eff}=3/16\times C_L$



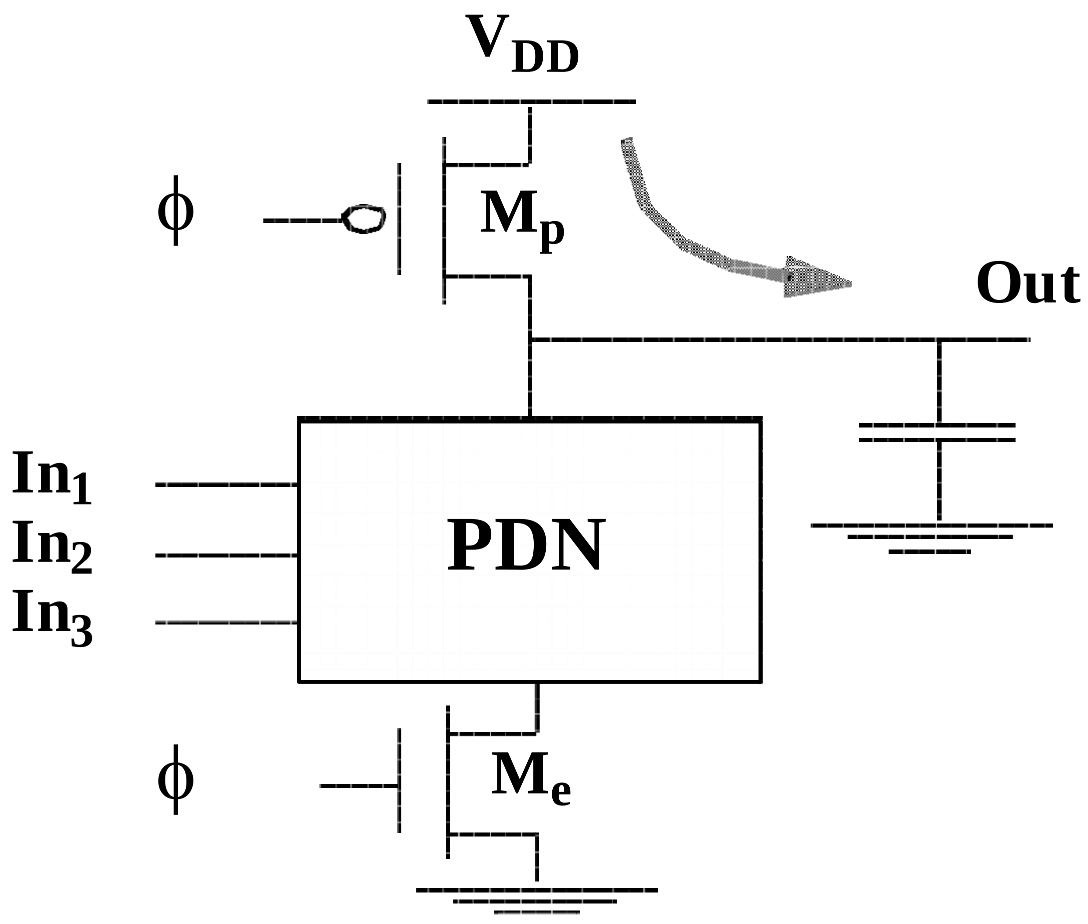
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of 2 input NOR gate

SWITCHING ACTIVITY REDUCTION (2/5)

Power Consumption is Data Dependent

Dynamic Circuit



Power is Only Dissipated when Out=0!

$$C_{EFF} = P(Out=0).C_L$$

SWITCHING ACTIVITY REDUCTION (3/5)

Power Consumption is Data Dependent

- Dynamic Circuit
  - Example 2: 2 input dynamic NOR gate

    Assume P(A=1)=1/2, P(B=1)=1/2.

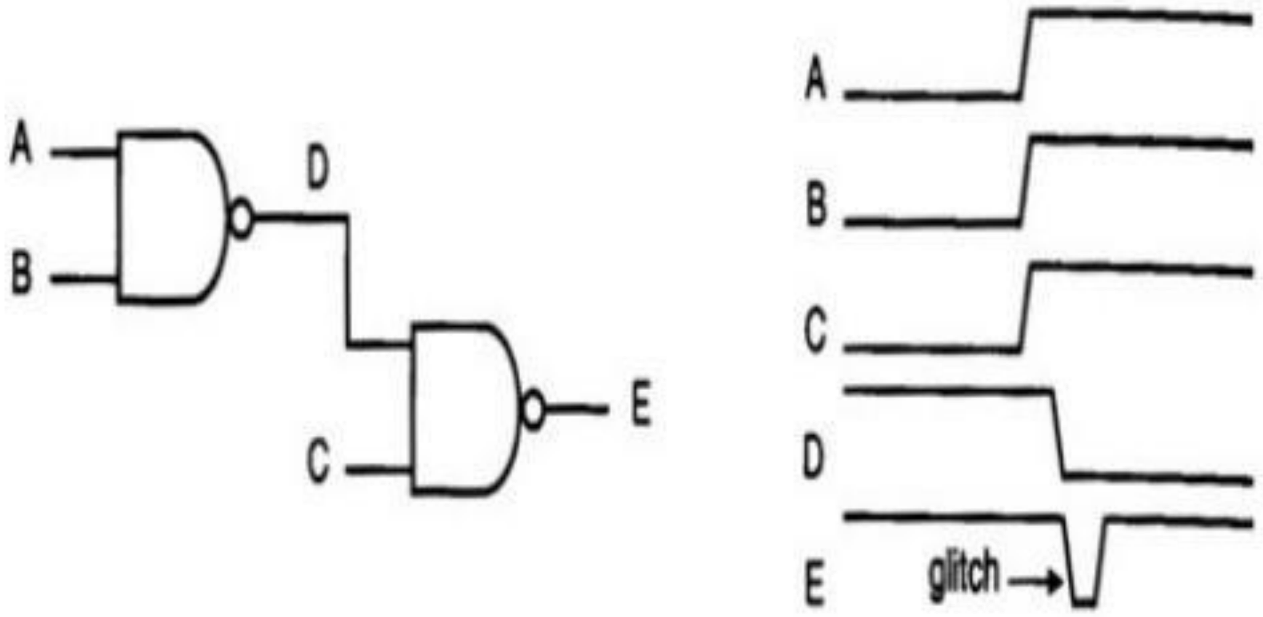
    P(out=0)=3/4

    $\boldsymbol{C_{eff}=3/4 \times C_L}$

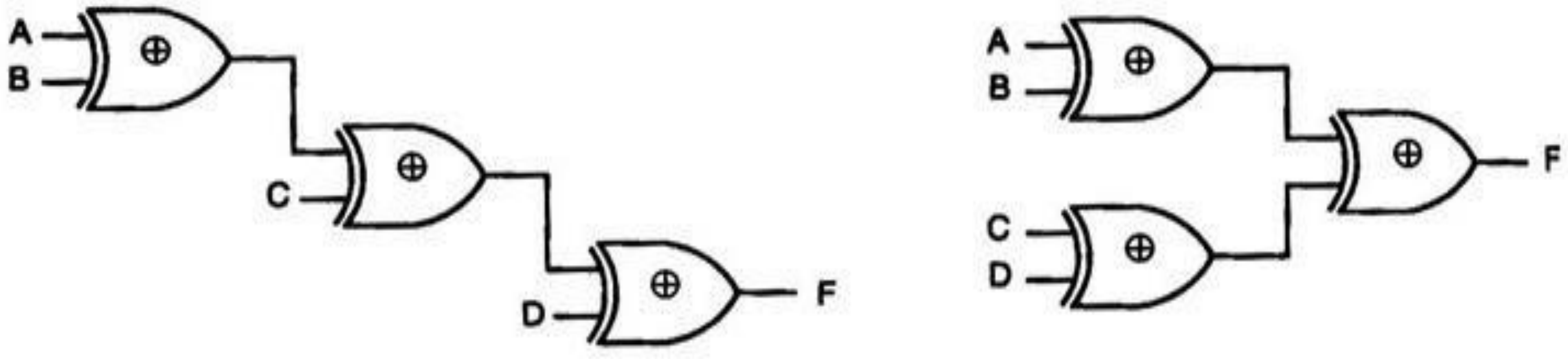
Switching activity is always higher in dynamic circuits

SWITCHING ACTIVITY REDUCTION (4/5)
GLITCH REDUCTION

- Dynamic hazards
  - –Caused by unbalanced delays
  - –Usually 8% - 25% of dynamic power
- Suspicious for glitches
  - –Deep logic depth
  - –Ripple of carry in adder
- Relief
  - –Equalize lengths of timing paths through design.
  - –Reduce logic depth: Pipelining



Signal glitching in multi-level static CMOS circuits.



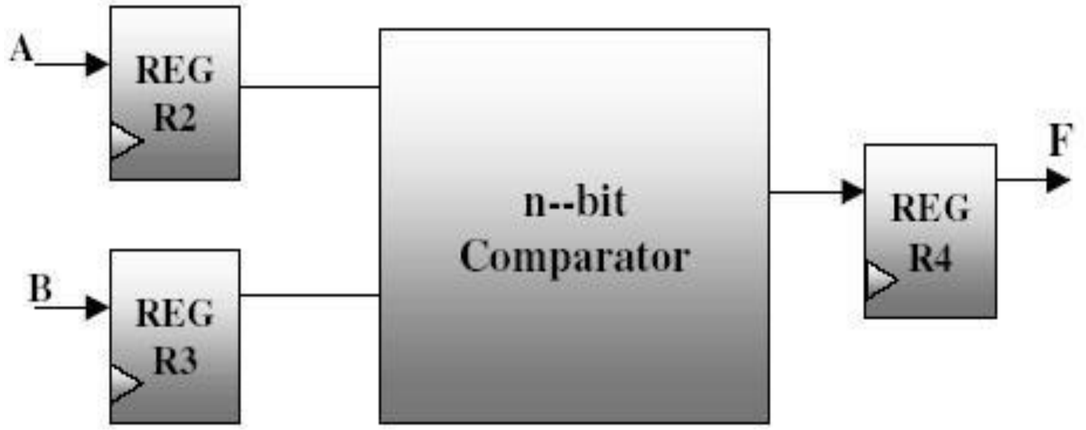
(a)

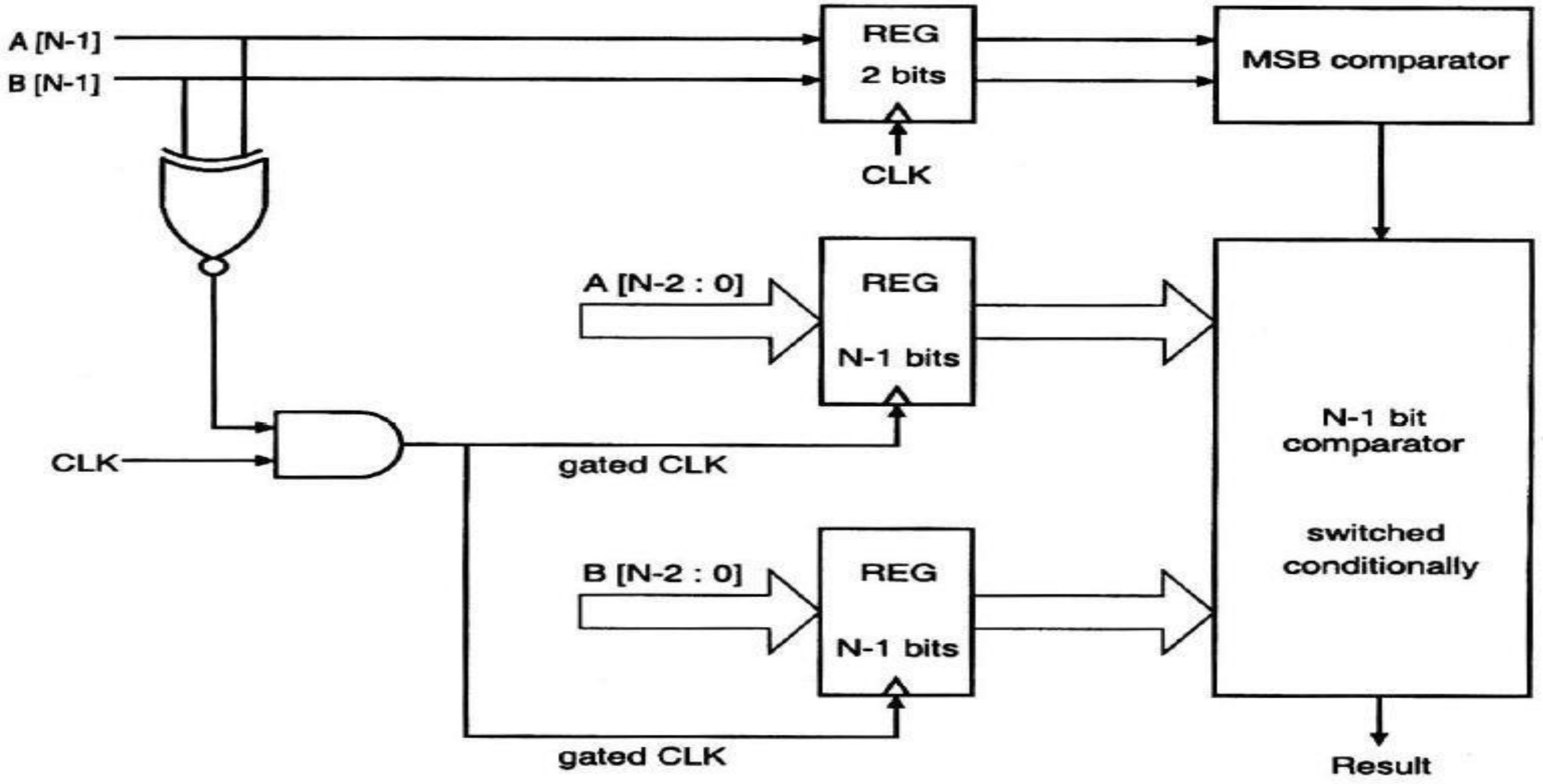
(b)

(a) Implementation of a four-input parity (XOR) function using a chain structure. (b) Implementation of the same function using a tree structure which will reduce glitching transitions.

SWITCHING ACTIVITY REDUCTION (5/5)
PRE-COMPUTATION TECHNIQUE

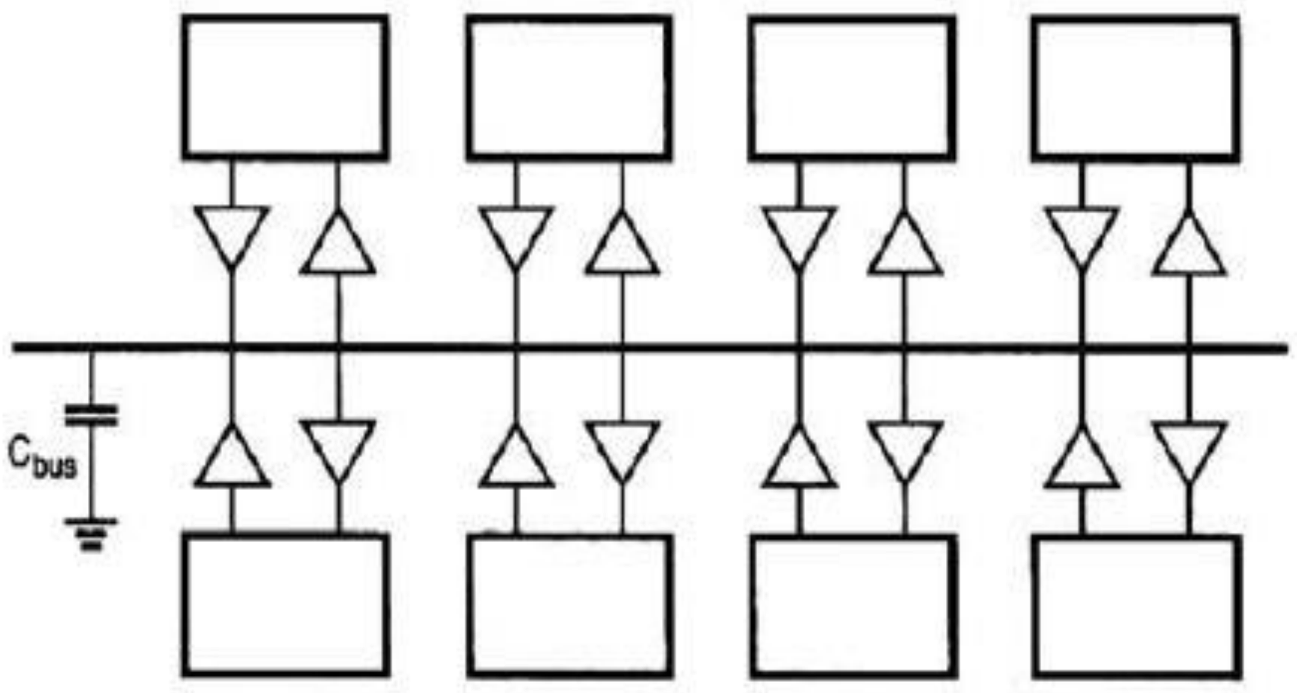
- Saves power by not enabling registers R2 and R3 in half (50%) of cases



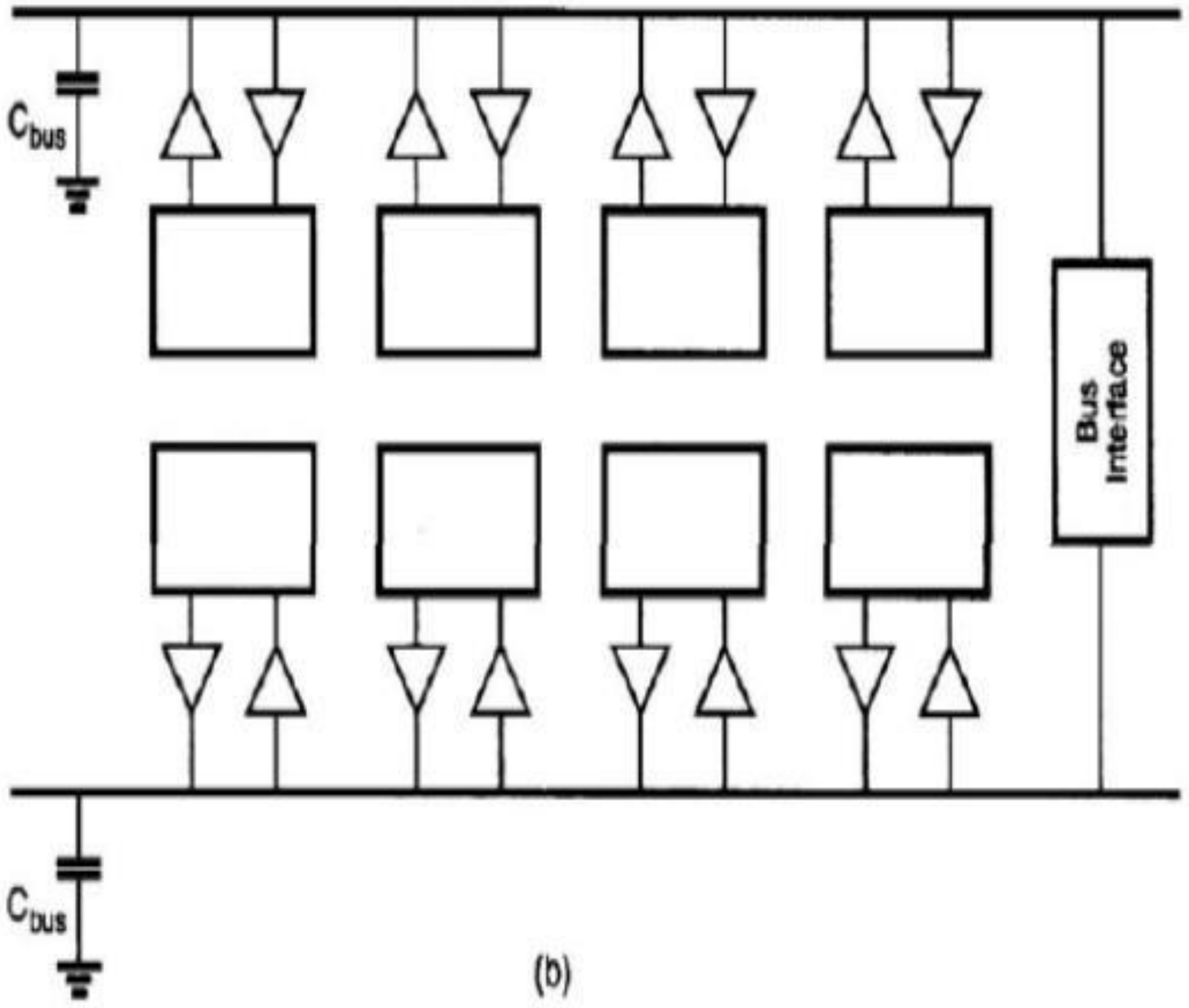


REDUCTION OF SWITCHED CAPACITANCE

- Resource Sharing
  - –Causes switching overhead
  - –Increases effective capacitance
- Global buses vs. Local interconnect
- Locality: Shorter wires



(a)



(b)

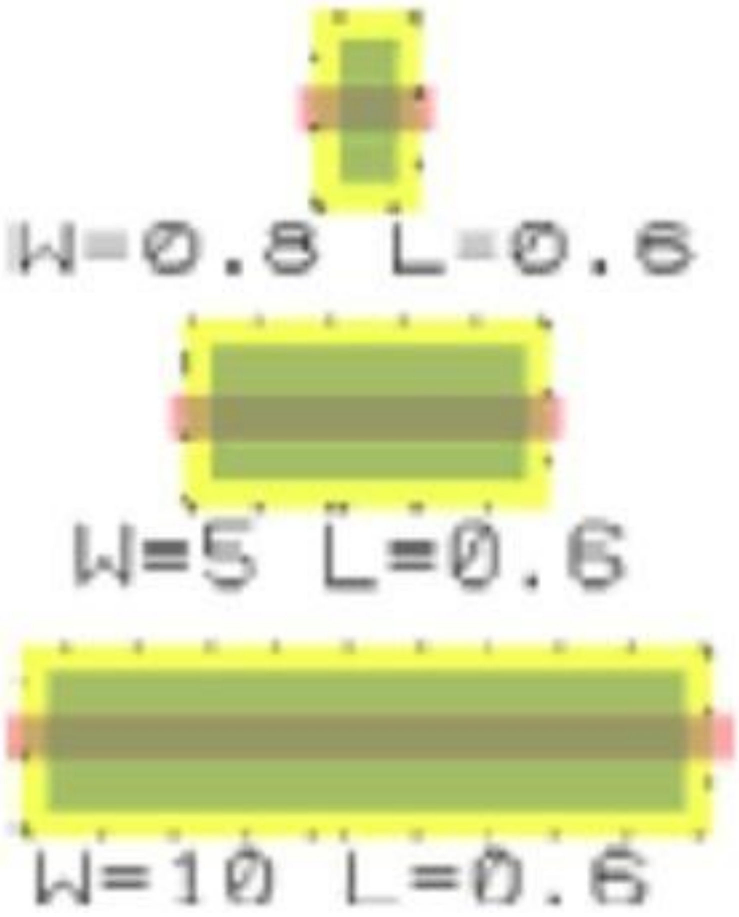
REDUCTION OF SWITCHED CAPACITANCE

Use Minimal Transistor Where Possible

- Transistor width W
  - –Current driving capability

    $I_D = K \times (W/L) \times ......$
  - –Capacitance

    $C = C_{OX} \times W \times L$
  - –Large W
    - For dominating interconnect
- Minimum transistors
  - –Lowest capacitance
  - –Optimal for low power



DESIGN FOR LOW POWER (CONT.)

- **Process Technology**
  - **V_{DD}** reduction
  - Threshold voltage
    - High threshold voltage
    - Double-threshold devices
      - Low threshold for high speed
      - High threshold for low power
  - Silicon on insulator (SOI)

ASSESSMENT

1.List out the source of leakage current

2. P_{total} = P------+P---------+$P_{------------}$ +$P_{-----------}$

3. Pdynamic = CL × ------× f

4.List out the Variable-threshold CMOS (VTCMOS) Circuits Vs Multiple-threshold CMOS (MTCMOS) Circuits

5.Switching activity is always ---------(higher/lower) in dynamic circuits

6.How can you reduce glitches.

SUMMARY & THANK YOU

- Power consumption
- Dynamic, Short circuit, Leakage, Static Design for low power
- Motivation for VLSI innovation
- On all levels! System level … process tech. Lowest possible

Supply voltage $\mathbf{V_{DD}}$
Effective capacitance $\mathbf{C_{eff}}$
Clock frequency $\mathbf{f_{CLK}}$