SNS COLLEGE OF ENGINEERING

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF CSE (IoT)

23ITT201 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

II YEAR/ III SEMESTER

UNIT 1 – **COMBINATIONAL LOGIC**

TOPIC –BINARY ADDER

BINARY ADDER

Alternate name

ADDITION

3	1	4	8
+ 8	+ 3	+ 4	+ 6
6	8	8	5
+ 6	+ 3	+ 2	+ 6
7	3	7	2
+ 8	+ 0	+ 6	+ 3
9	6	3	4
+ 3	+ 5	+ 3	+ 5

PARALLEL ADDER

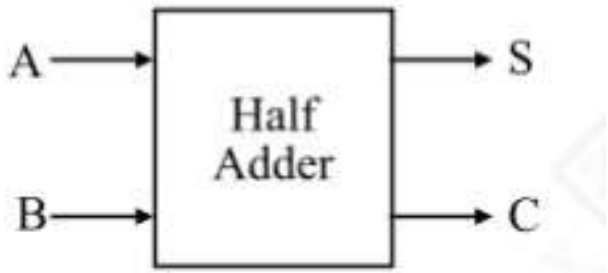
Alternate name

RIPPLE ADDER

For reference

Half adder:

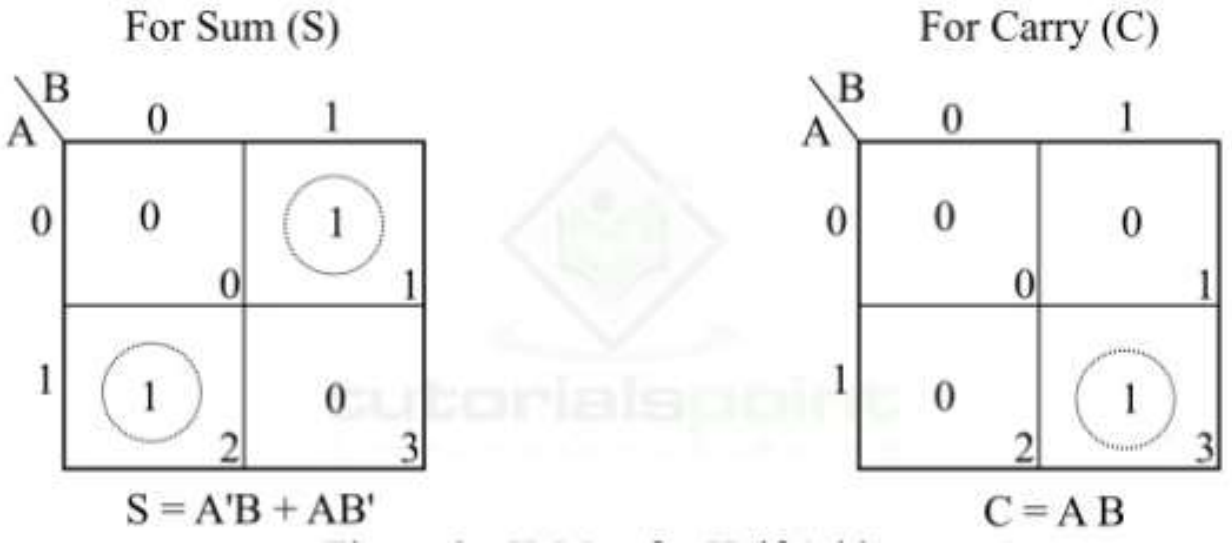
- A combinational logic circuit which is designed to add two binary digits is called as a **half adder**. The half adder provides the output along with a carry value (if any)



Half adder- Truth Table

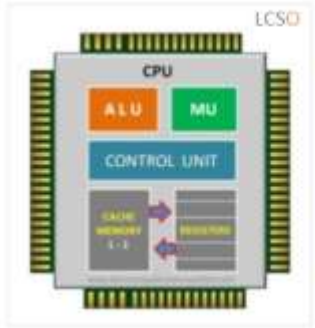
Inputs		Outputs	
A	B	S (Sum)	C (Carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

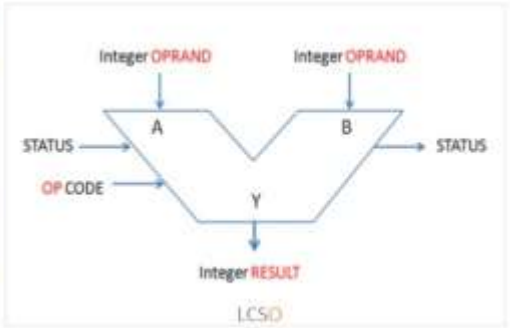
K- map for Half adder



Applications of Half adder

- Half adder is used in **ALU (Arithmetic Logic Unit) of computer processors** to add binary bits.





- Half adder is used **to realize full adder circuit**.
- Half adder is used in **calculators**.
- Half adder is used to **calculate addresses and tables**.

Activity Time!!!

Lets have fun with

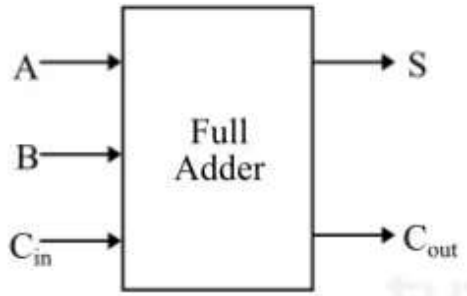
COLOURS ☺

RED	PINK	YELLOW	GREEN
ORANGE	BROWN	VOILET	WHITE
GRAY	BLUE	BROWN	RED
YELLOW	ORANGE	WHITE	BLUE
PINK	GRAY	RED	GREEN

For reference

Full adder:

- A combinational circuit which is designed **to add three binary digits** and produces two outputs (sum and carry) is known as a full adder.
- Thus, a full adder circuit adds three binary digits, where two are the inputs and one is the carry forwarded from the previous addition.



Block Diagram

Full adder- Truth Table

Inputs			Outputs	
A	B	C_{in}	S (Sum)	C_{out} (Carry)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Hence, from the truth table, it is clear that the sum output of the full adder is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1.
- While the carry output has a carry of 1 if two or three inputs are equal to 1.

K- map for Full adder

For Sum (S)

A \ BC_{in}	00	01	11	10
0	0 (0)	1 (1)	0 (3)	1 (2)
1	1 (4)	0 (5)	1 (7)	0 (6)

$S = A'B'C_{in} + A'BC'_{in} + AB'C'_{in} + ABC_{in}$

For Output Carry (C_{out})

A \ BC_{in}	00	01	11	10
0	0 (0)	0 (1)	1 (3)	0 (2)
1	0 (4)	1 (5)	1 (7)	1 (6)

$C_{out} = AB + AC_{in} + BC_{in}$

Advantages of full adder

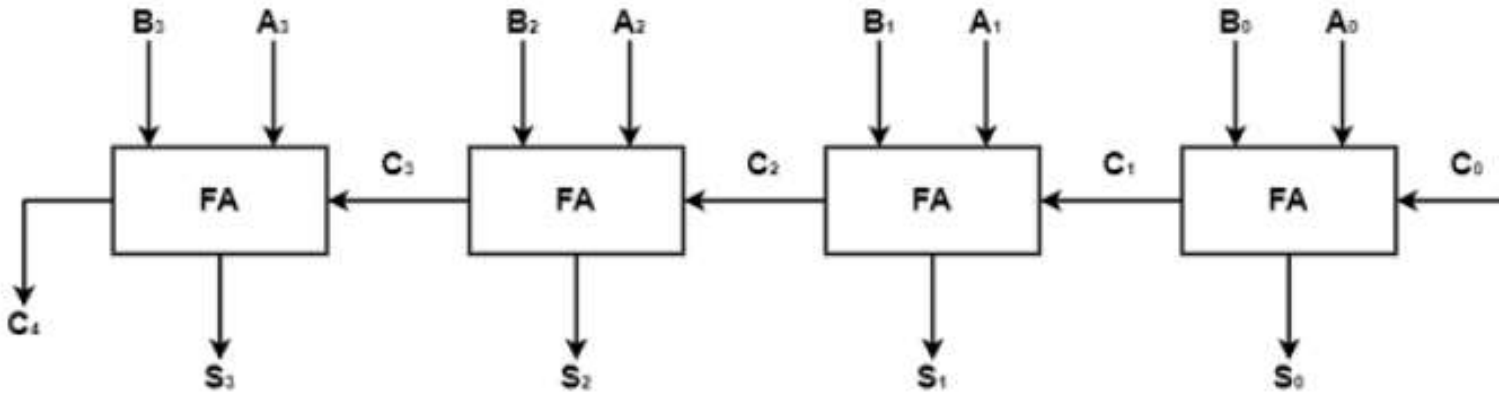
- Full adder provides facility to add the carry from the previous stage.
- The power consumed by the full adder is relatively less as compared to half adder.
- Full adder can be easily converted into a half subtractor just by adding a NOT gate in the circuit.
- Full adder produces higher output that half adder.
- Full adder is one of the essential part of critic digital circuits like multiplexers.
- Full adder performs operation at higher speed.

Applications of full adder

- Full adders are used in ALUs (arithmetic logic units) of CPUs of computers.
- Full adders are used in calculators.
- Full adders also help in carrying out multiplication of binary numbers.
- Full adders are also used to realize critic digital circuits like multiplexers.
- Full adders are used to generate memory addresses.
- Full adders are also used in generation of program counterpoints.
- Full adders are also used in GPU (Graphical Processing Unit).

BINARY ADDER

- A Binary Adder is a digital circuit that implements the **arithmetic sum of two binary numbers** supported **with any length** is known as a binary adder.
- It is generated using **full-adder circuits connected in sequence**. The output carries from one full-adder linked to the input carry of the next full-adder.



4-Bit Binary Adder

BINARY ADDER

- The **augend bits of A** and the **addend bits of B** is created by subscript numbers from right to left, with subscript 0 indicating the low-order bit. The carries are linked in a chain by the **full-adders**.
- The input carry to the binary adder is C_0 and the output carry is C_4. The S outputs of the full-adders create the needed sum bits.
- An **n-bit binary adder** is needed **n full-adders**.
- The output carries from each full-adder is linked to the input carry of the next-high-order full-adder.
- The n data bits for the A inputs come from one register including R1, and the n data bits for the B inputs come from another register including R2. The sum can be transferred to a third register or one of the source registers (R 1 or R2), restoring its earlier content.

SUMMARY

Thank You!