SNS COLLEGE OF ENGINEERING

Coimbatore-35
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DEPARTMENT OF CSE (IoT)

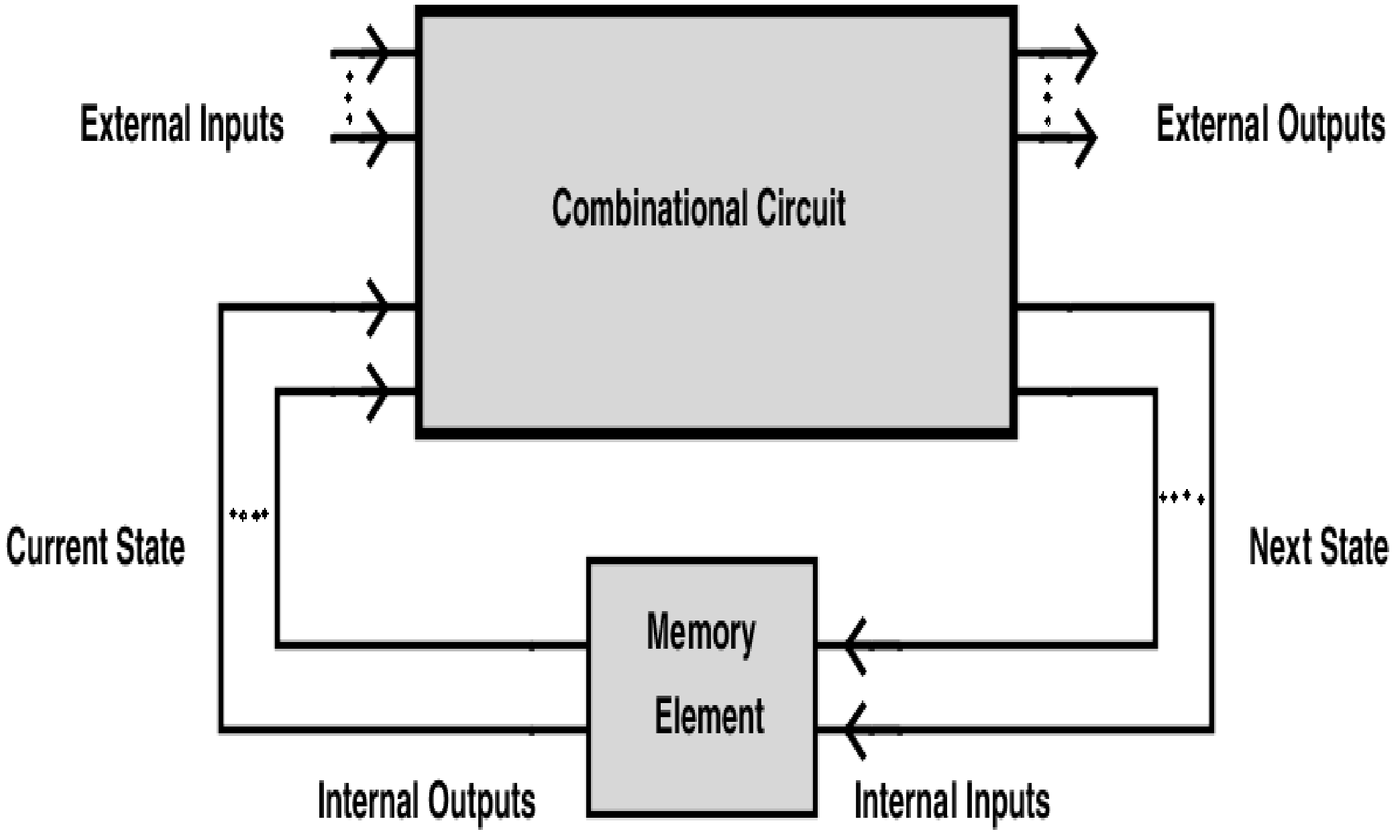
23ITT201 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

II YEAR/ III SEMESTER

UNIT 2 – **SYNCHONOUS SEQUENTIAL LOGIC**

TOPIC –LATCHES

SEQUENTIAL CIRCUITS



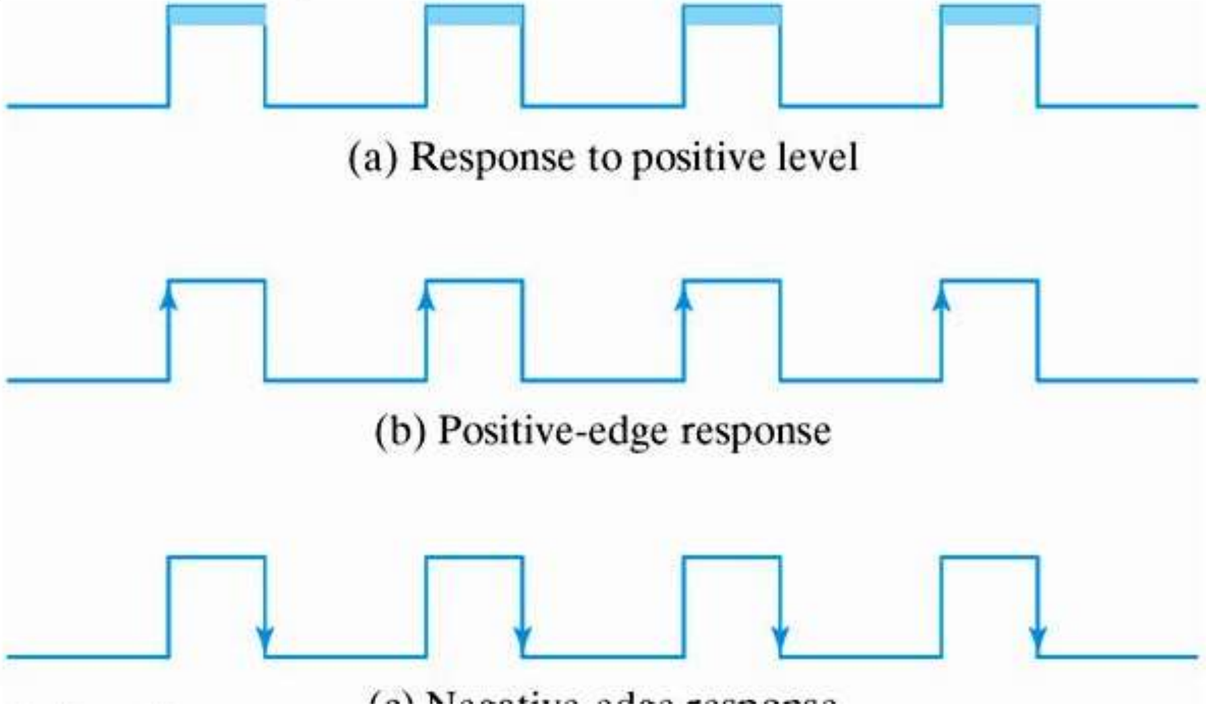
SEQUENTIAL CIRCUITS

- This sequential circuit contains a set of inputs and outputs
- The outputs of sequential circuit depends not only on the combination of present inputs but also on the previous outputs
- Previous output is nothing but the **present state**
- Therefore, sequential circuits contain combinational circuits along with memory storage elements
- Some sequential circuits may not contain combinational circuits, but only memory elements

LATCH

- LATCH –building block of sequential circuits capable of storing one bit information
- It has 2 output states Q and Q Complement
- It is built from Logic gates
- Latches does not have Clock signal instead it have enable line
- Output changes only when enable input signal is applied
- Latch is level Triggered

- A trigger
  - The state of a latch or flip-flop is switched by a change of the control input
- Level triggered – latches
- Edge triggered – flip-flops

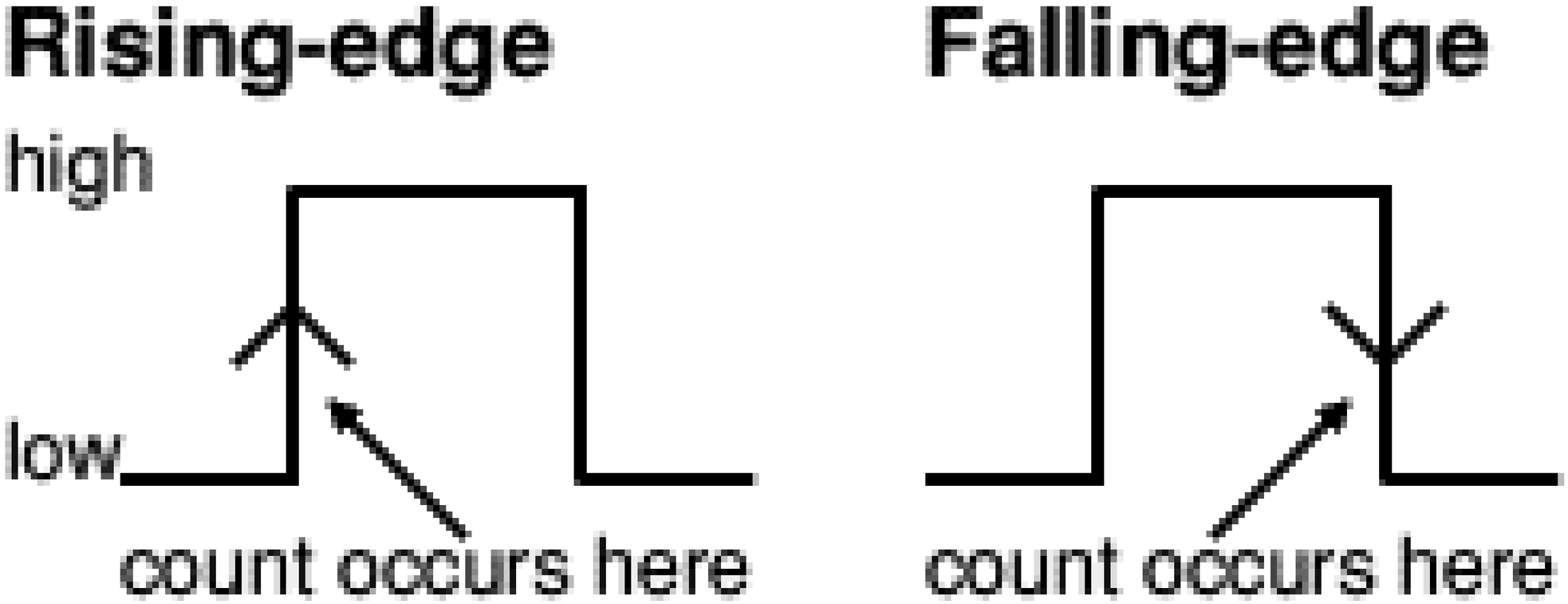


(a) Response to positive level

(b) Positive-edge response

. 5.8

EDGE TRIGGERING



Level Triggering	Edge Triggering
1. It is of two types – High level triggering – Low level triggering	1. It is of two types : – Positive edge triggering – Negative edge triggering
2. The latch or flip-flop circuits which change their outputs only corresponding to active high or low levels are called as level triggered latches or flip-flops.	2. Those flip-flops which change their outputs only corresponding to the positive or negative edge of the clock input are called as edge triggered flip-flops.

TYPES OF LATCH

1.SR Latch

R=Reset and S=Set

2.D Latch

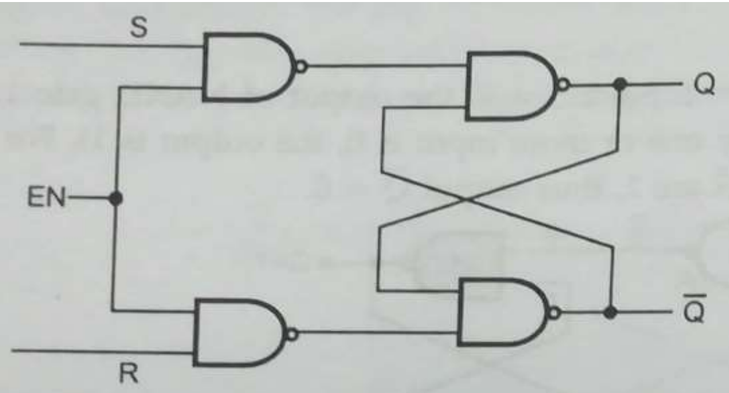
D means Delay

3.T Latch

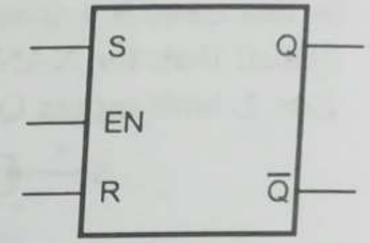
T means Toggle

4.JK Latch

SR LATCH



(a) SR latch with enable input using NAND gates



(b) Logic symbol

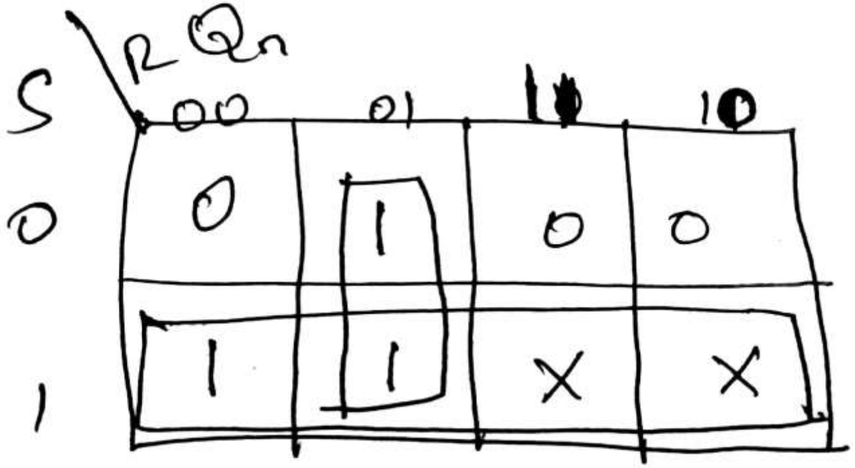
Fig. 6.7

EN	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Indeterminate
1	1	1	1	X	
0	X	X	0	0	No change (NC)
0	X	X	1	1	

Table 6.2 Truth table for SR latch with enable input

SR LATCH

Characteristics Equation



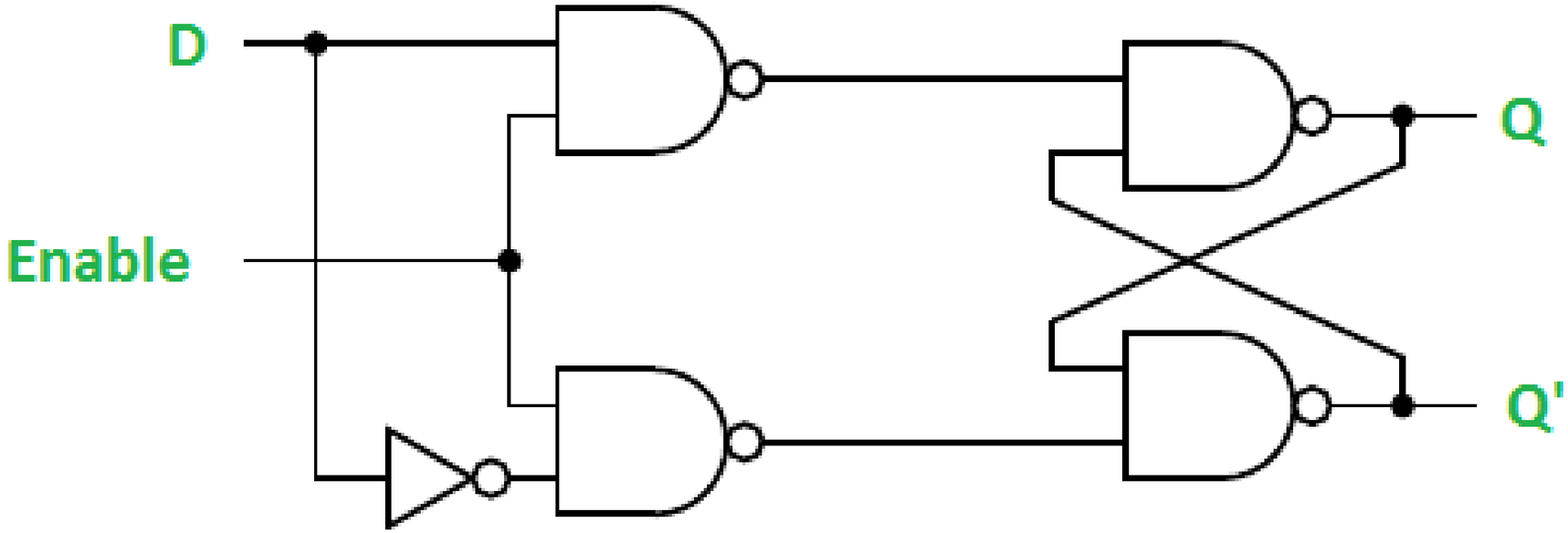
$$Q_{n+1} = S + \bar{R} Q_n$$

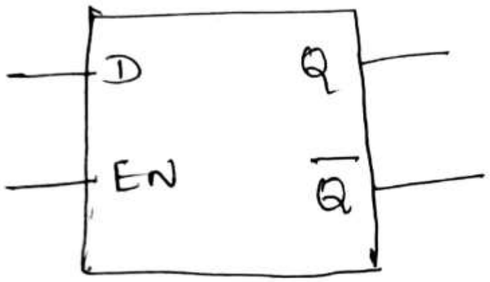
SR LATCH

Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D LATCH





Logic Symbol.

Truth Table

E	D	Q_n	Q_{n+1}
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1
0	X	0	0
0	X	1	1

Characteristic Equation

D \ Q_n	0	1
0	0	0
1	1	1

$$Q_{n+1} = D$$

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

ADVANTAGES OF LATCHES

- The advantages of latches include the following.
- The designing of latches is very flexible when we compare with FFs (flip-flops)
- The latches utilize less power.
- The performance of latch in the design of the high-speed circuit is quick because these are asynchronous within the design and there is no need of CLK signal.
- The shape of the latch is very small and occupies less area
- If the operation of latch based circuit is not finished in a set time, they borrow the necessary time from other to complete the operation
- Latches give aggressive clocking when contrasted with flip-flop circuits.

APPLICATIONS OF LATCHES

- The applications of latches include the following.
- Generally, latches are used to keep the conditions of the bits to encode binary numbers
- Latches are single bit storage elements which are widely used in computing as well as data storage.
- Latches are used in the circuits like power gating & clock as a storage device.
- D latches are applicable for asynchronous systems like input or output ports.
- Data latches are used in synchronous two-phase systems for reducing the transit count.

ASSESSMENTS

1.What is Latch?
2.List the types of latches.
3.Difference between level trigger and edge triggering.

THANK YOU