



SNS COLLEGE OF ENGINEERING

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

- DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

- 19EC505–VLSI DESIGN

- III YEAR/ V SEMESTER

1

UNIT 3 –SEQUENTIAL LOGIC CIRCUITS

TOPIC 6 & 7 –CLOCK STRATEGIES



OUTLINE



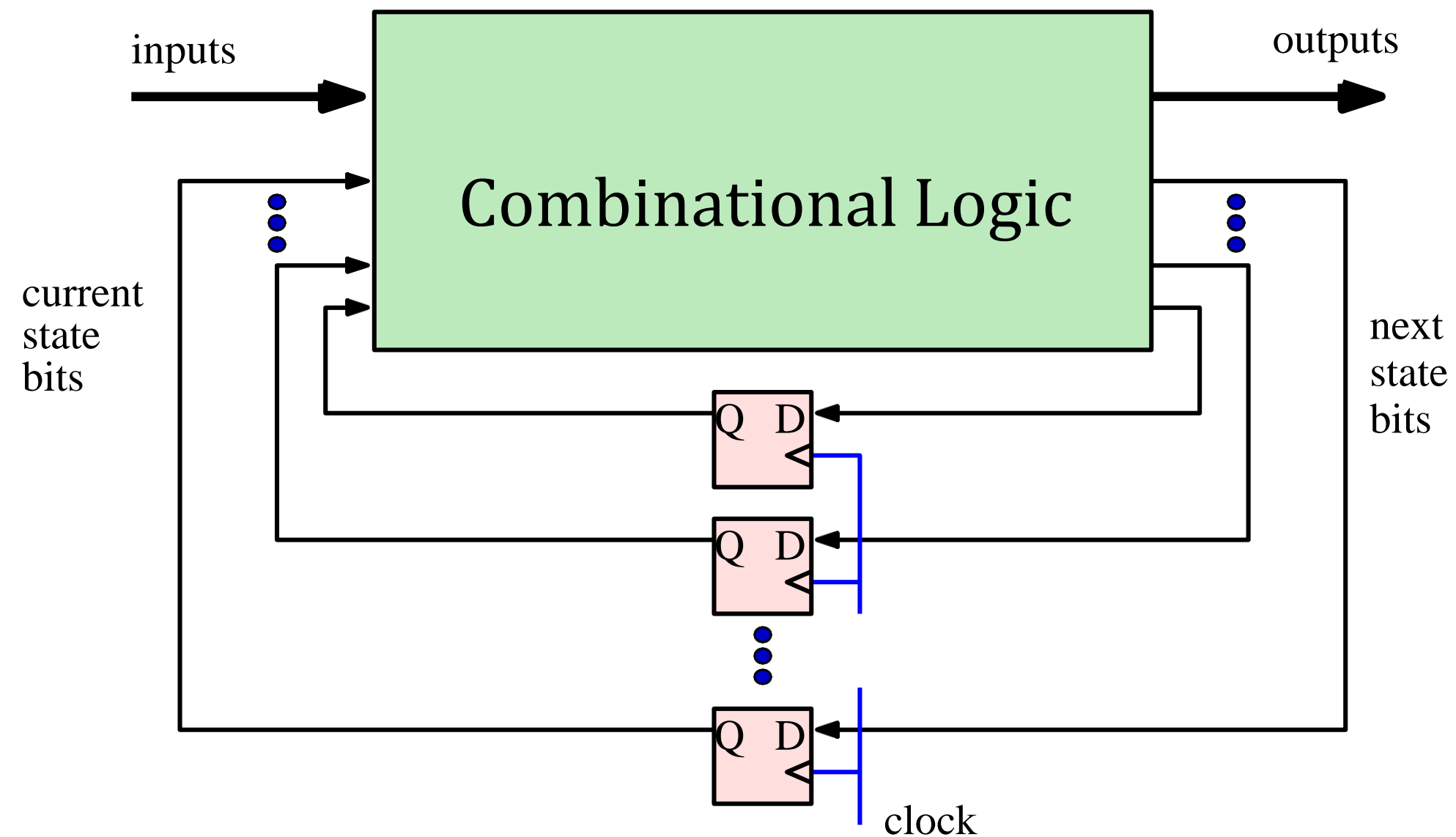
- INTRODUCTION
- CLOCKING STRATEGIES – *CLOCKED SYSTEMS*
- A SIMPLE FINITE STATE MACHINE
LATCHES AND REGISTERS
- SYSTEM TIMING-SETUP & HOLD TIME
- ACTIVITY
- D REGISTER
- CLOCK SKEW
- STRATEGIES–SKEW CLOCK PIPELINE
- DETDFF –LATCH 1 & 2
- ASYNCHRONOUSLY SETTABLE & RESETTABLE REGISTER
- DYNAMIC REGISTERS
- SINGLE CLOCK
- ASSESSMENT
- SUMMARY & THANK YOU



CLOCKING STRATEGIES – *CLOCKED SYSTEMS*

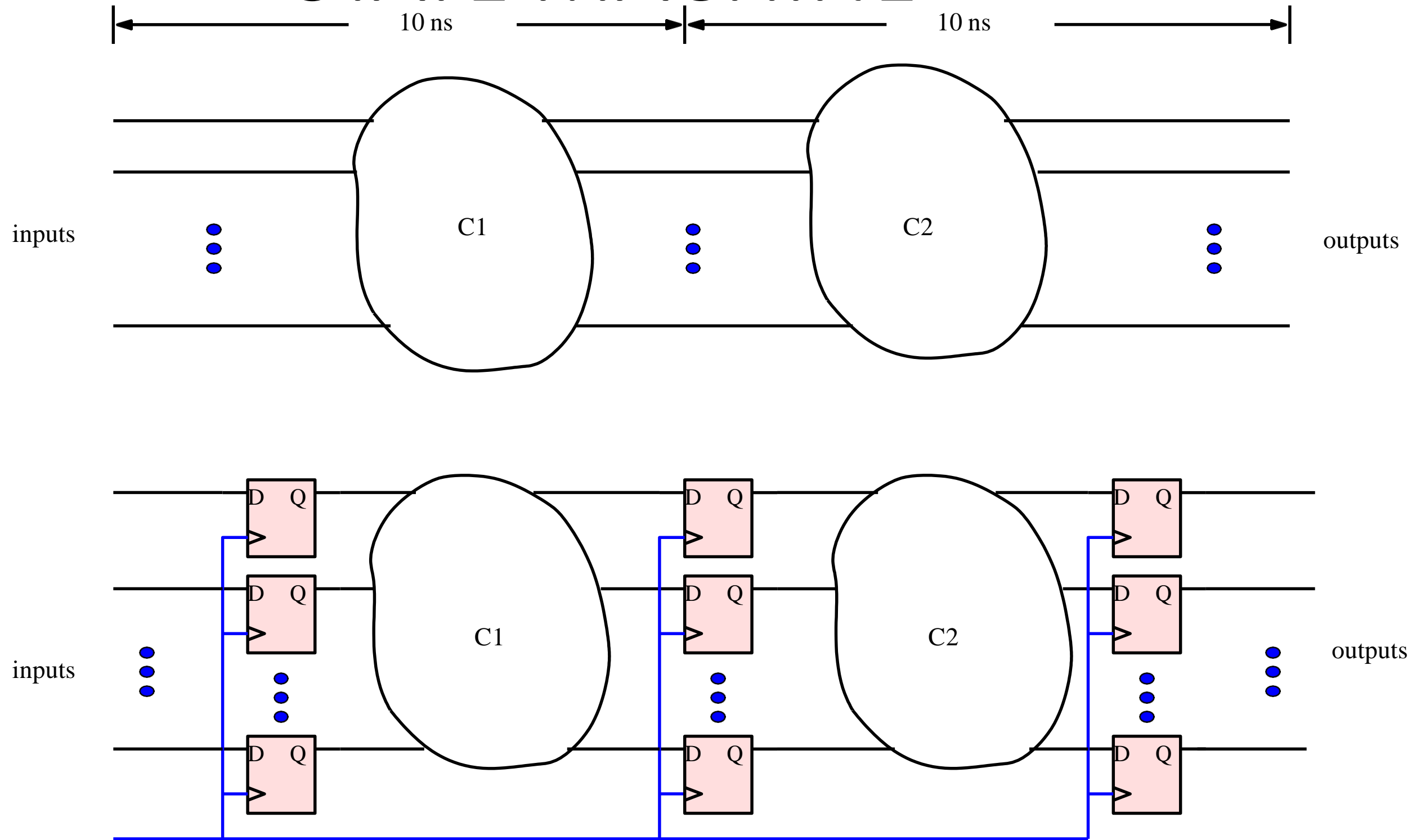


A SIMPLE FINITE STATE MACHINE



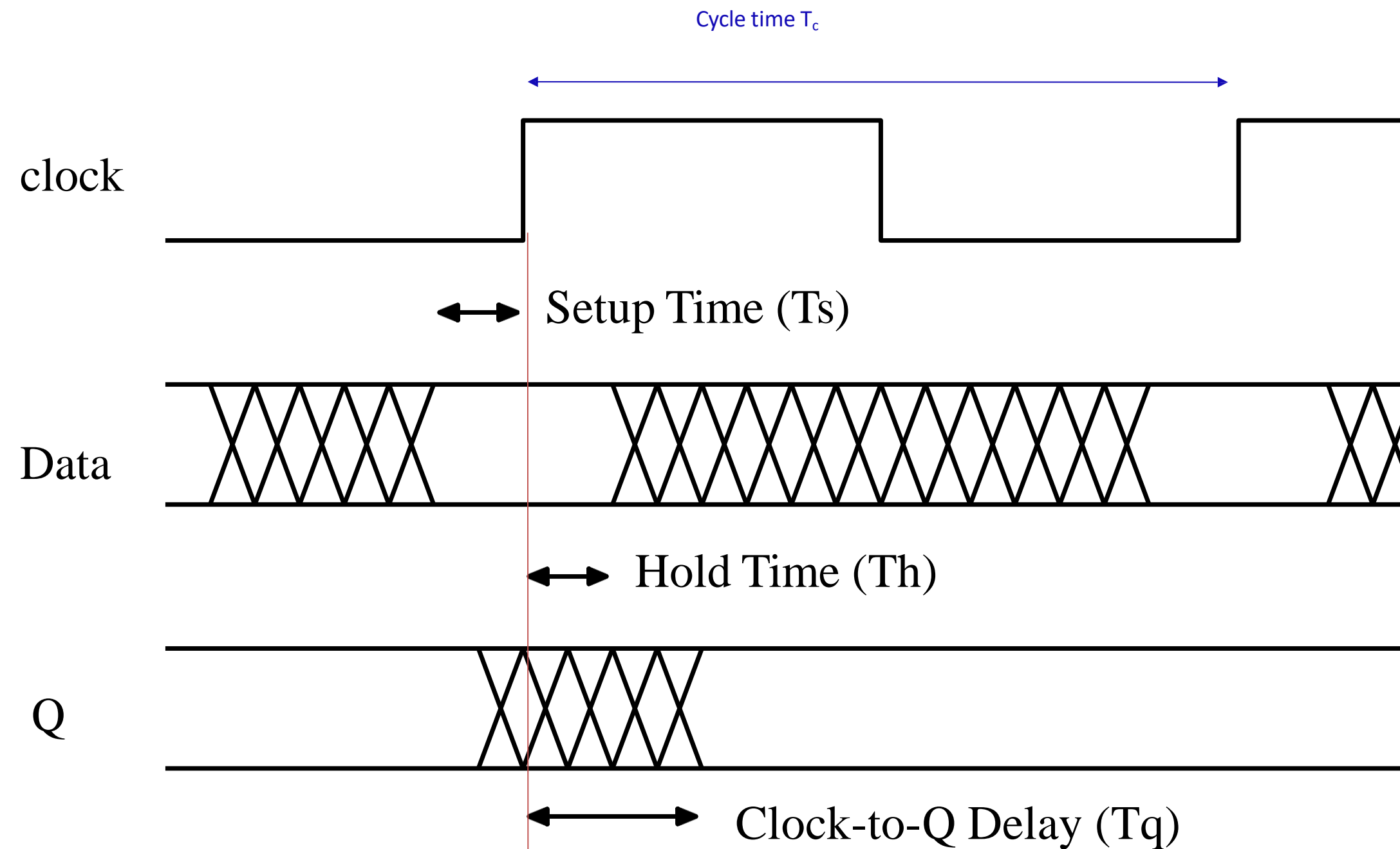


A SIMPLE FINITE STATE MACHINE



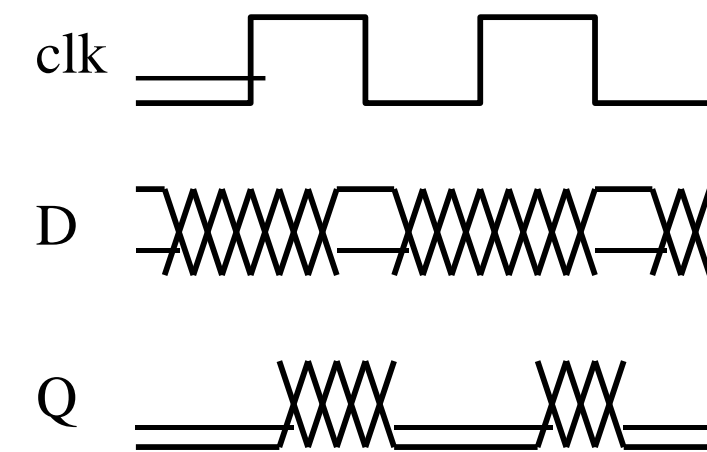
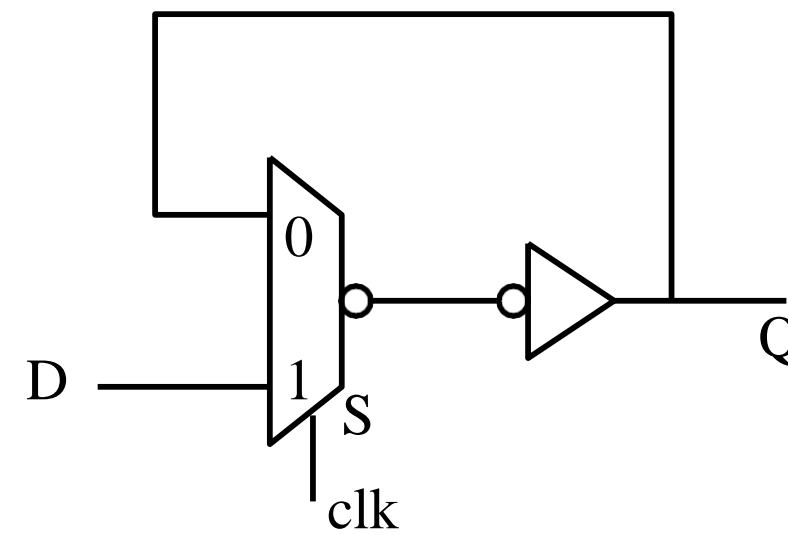
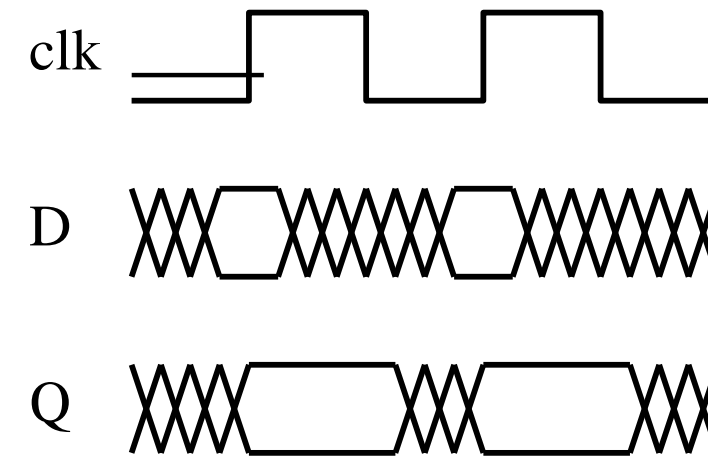
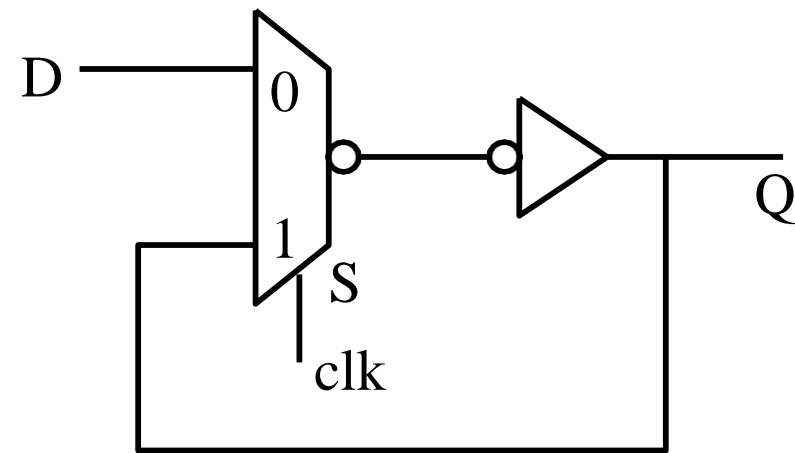


LATCHES AND REGISTERS



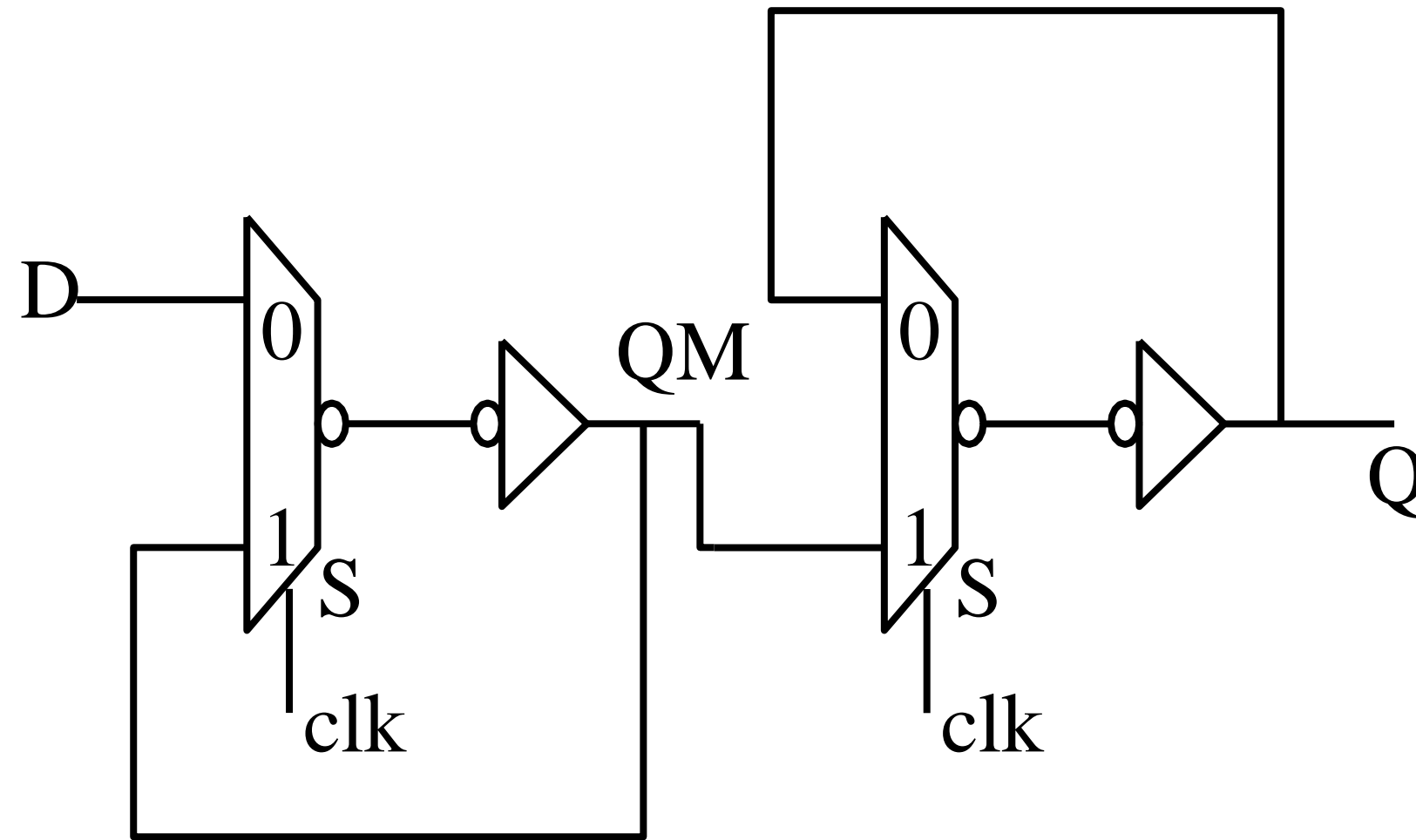


LATCHES



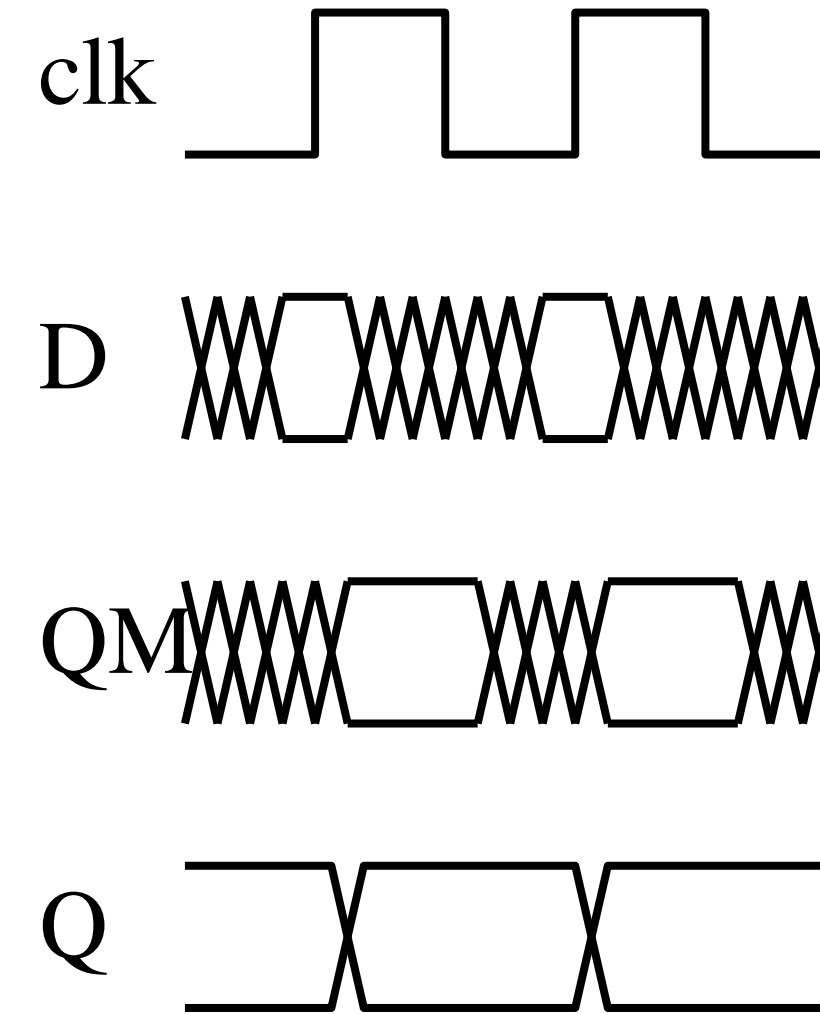


REGISTERS



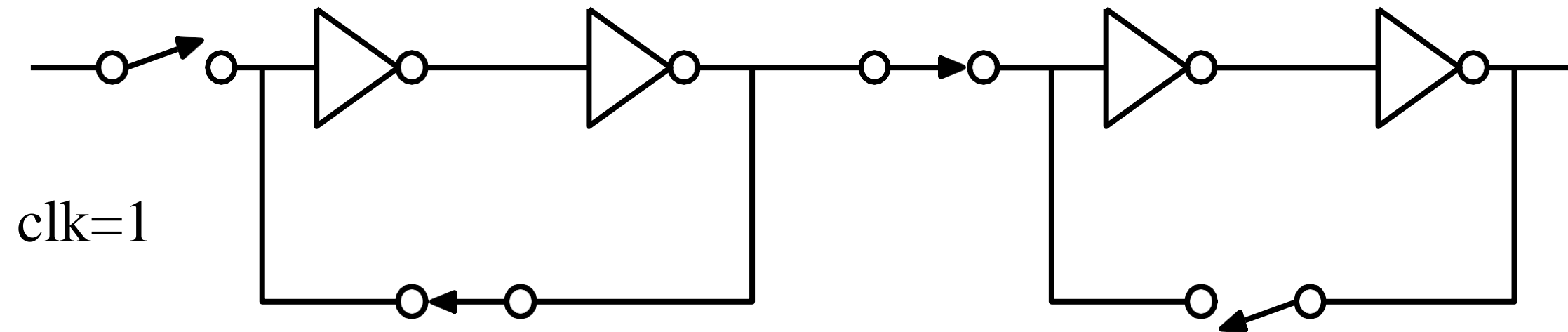
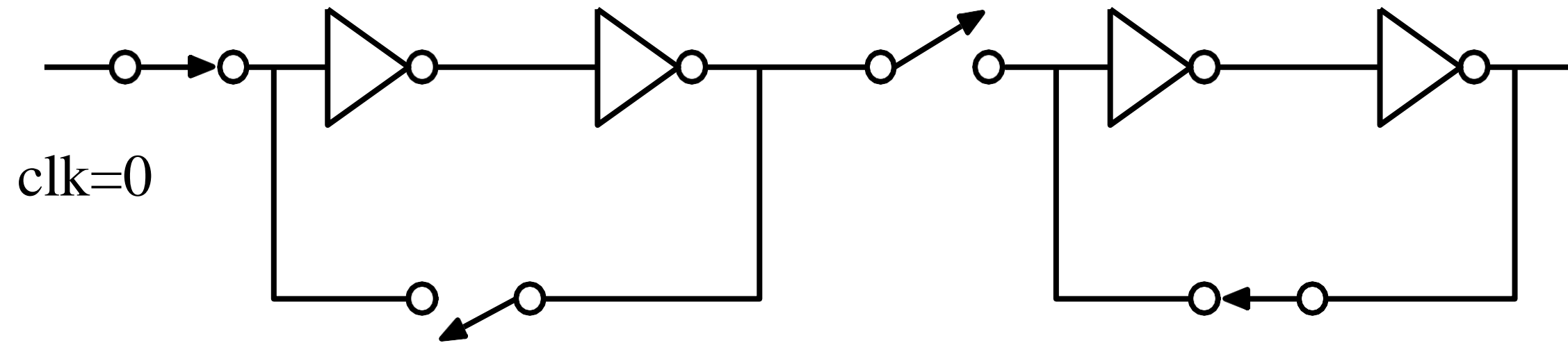
master

slave





REGISTERS

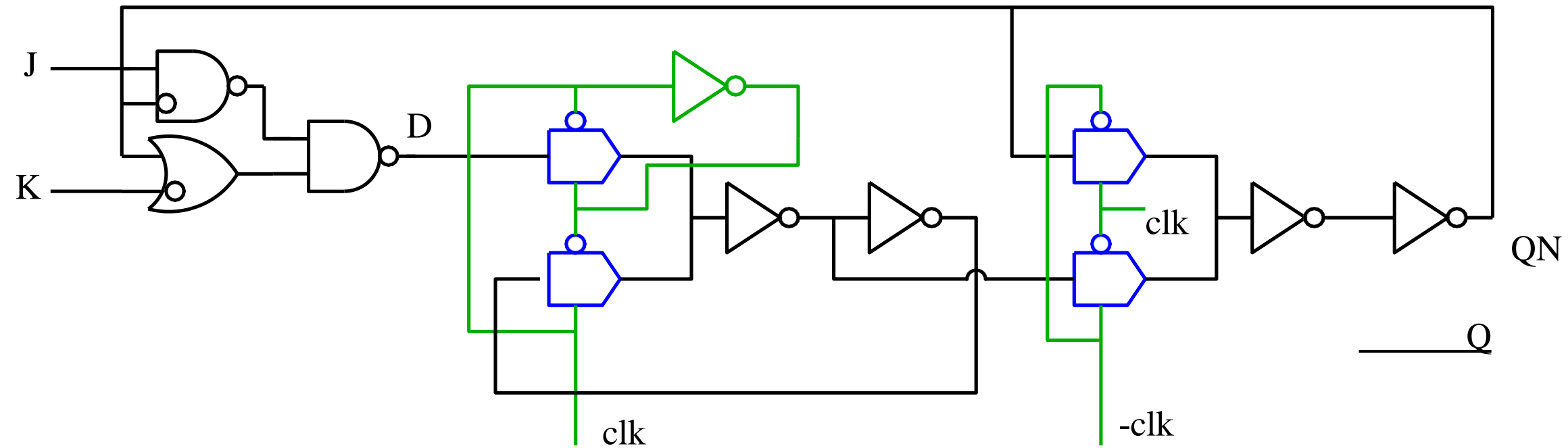


master

slave



CLOCKING STRATEGIES – JK REGISTERS

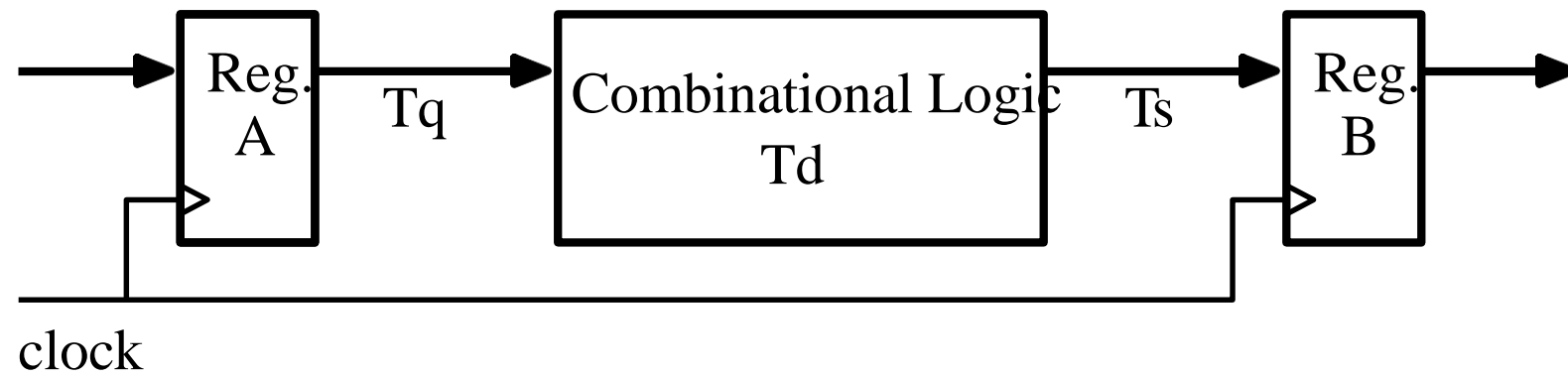


$J=K=0; Q=D$
 $JN=KN=1; A=QN, B=1; D=AN=Q$
 $J=0; K=1$
 $KN=0, JN=1; A=1, B=1; D=0$
 $J=1; K=0$
 $KN=1, JN=0; A=QN, B=Q; D=1;$
 $J=1; K=1$
 $KN=0, JN=0; A=1, B=Q; D=QN$

J	K	CLOCK	Q	QN
0	0	HI	Q	QN
0	1	HI	0	1
1	0	HI	1	0
1	1	HI	QN	Q



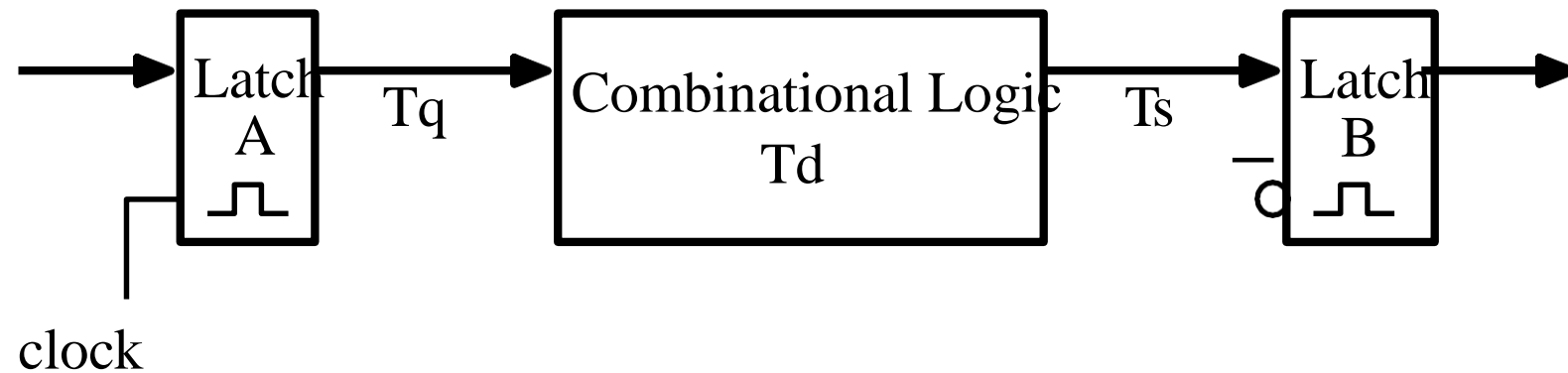
SYSTEM TIMING



$$T_{da} < T_{c1} - T_{qa} - T_{sb}$$

T_{qa} : the clock-to-Q time of latch A

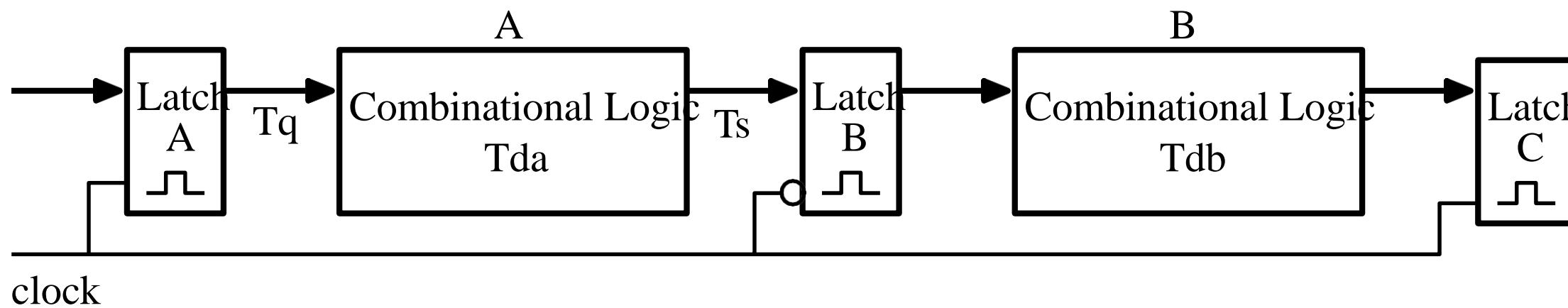
T_{sb} : the setup time of latch B



$$T_{db} < T_{c0} - T_{qb} - T_{sc}$$

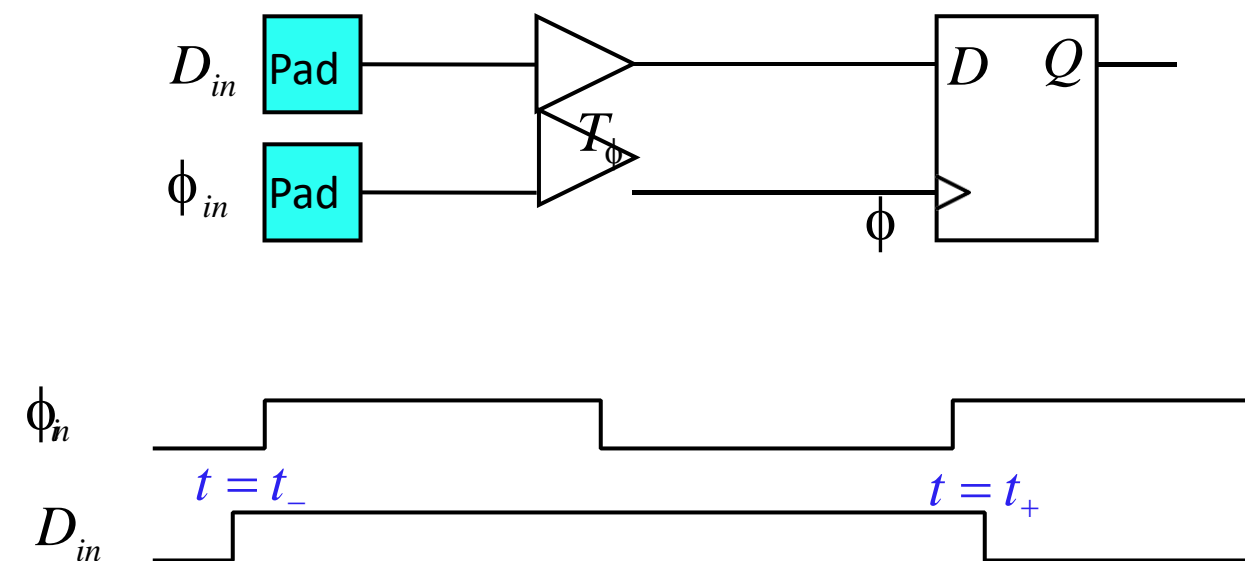
Finally,

$$T_c = T_{da} + T_{db} + 2[T_q + T_s]$$





SETUP & HOLD TIME



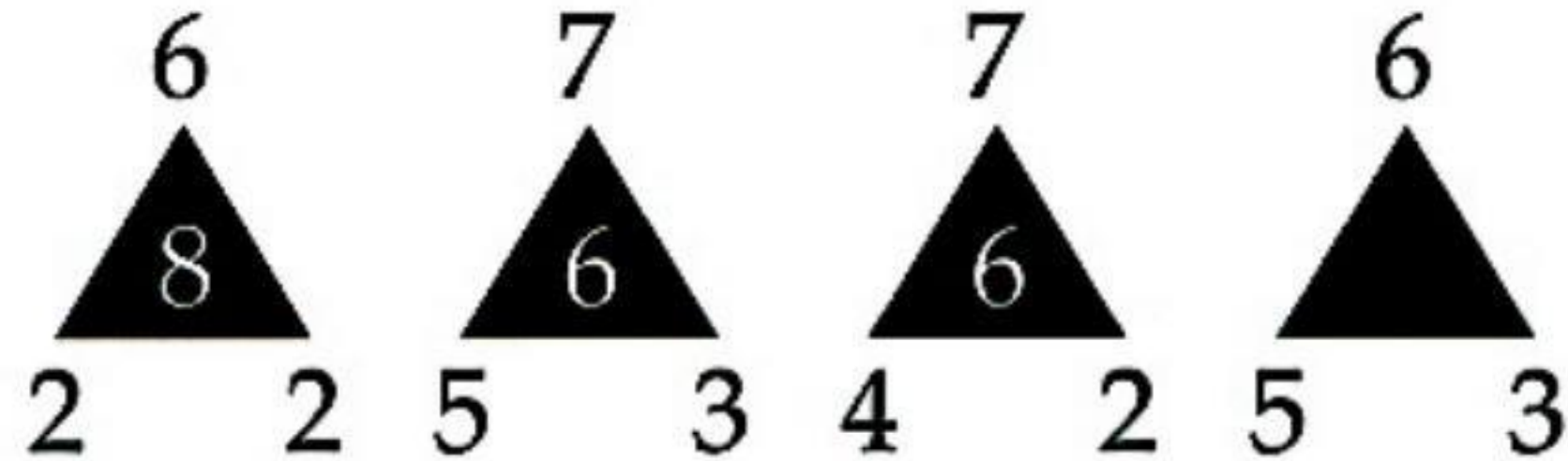
For an ideal DFF,

If D_{in} is high when $t = t_-$, then Q should be high

If D_{in} becomes to low when $t = t_+$, then Q still is high



CLASS ROOM ACTIVITY



Question:

Which figure should be placed in the empty triangle?

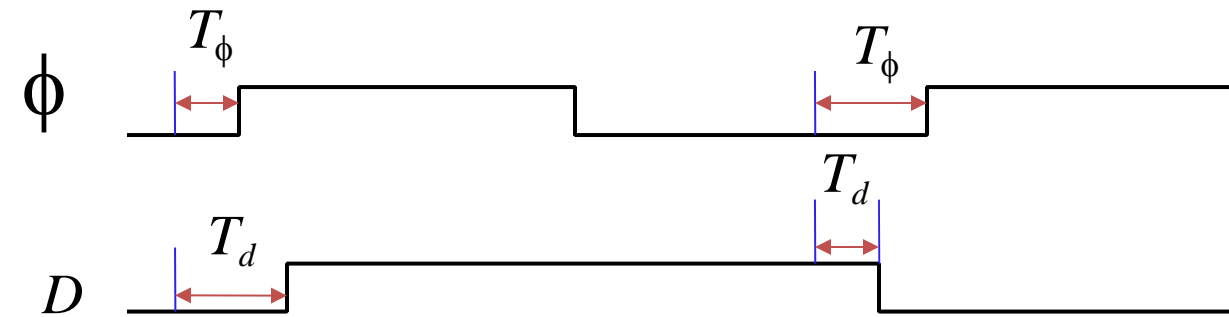
This puzzle works your executive functions in your frontal lobes by using your pattern recognition, hypothesis testing, and logic. Let us know how you do!



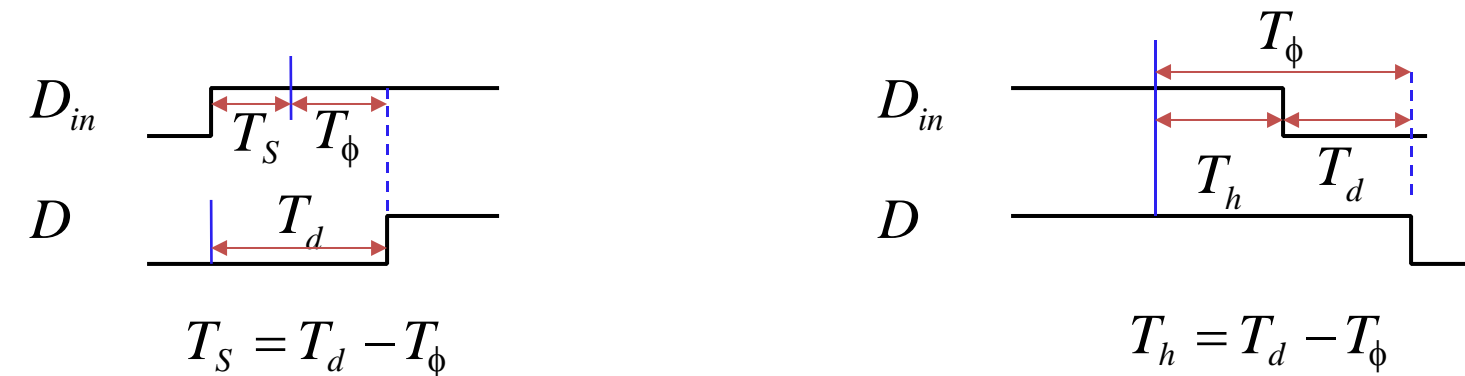
SETUP & HOLD TIME



When $T_d > T_\phi$, D_{in} should become high earlier and Q can become high



When $T_d < T_\phi$, D_{in} should retain at high longer and Q can be still at high

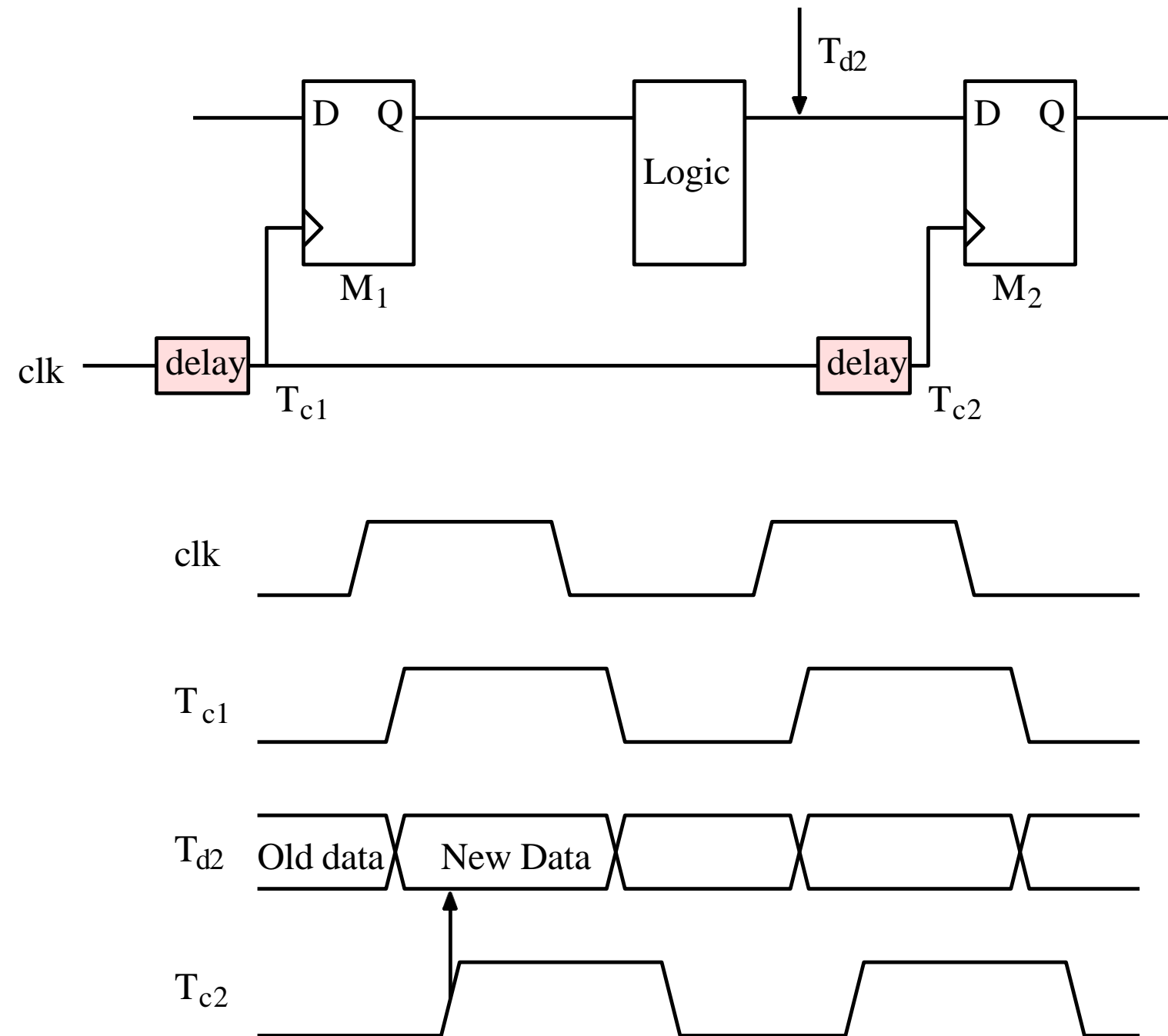


ANSWER: 3

SOLUTION:

The top number minus the bottom left-hand number is multiplied by the bottom right-hand number to give the number inside the triangle.

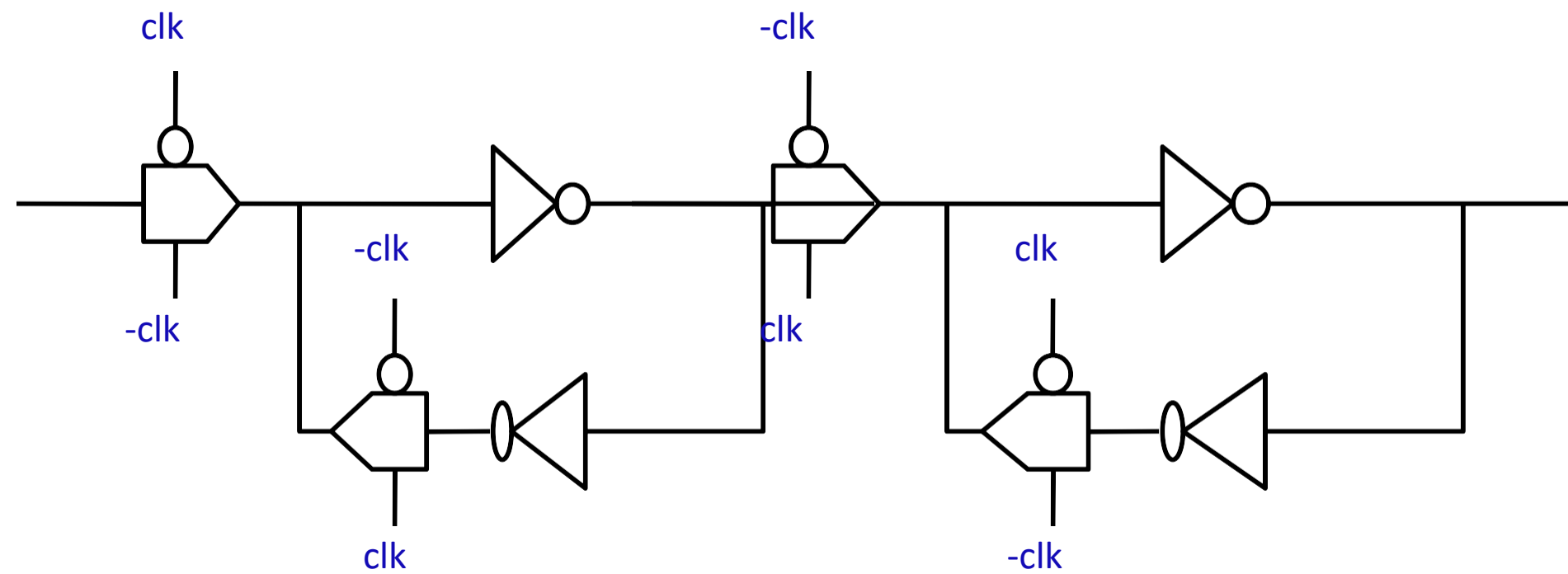
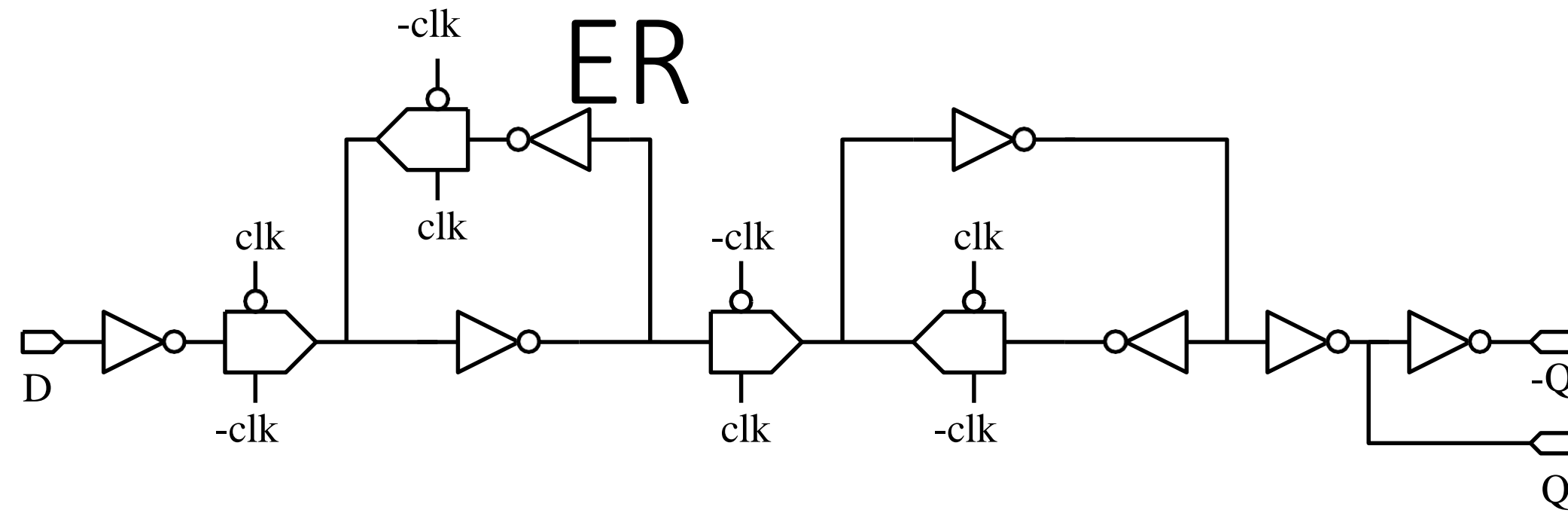
SETUP & HOLD TIME



1. When $T_{dc} > T_{dq} + T_{dl}$,
 M_2 latches
 the New data
 2. When $T_{dq} + T_{dl} - T_{dc} > T_C$,
 M_2
 latches Old data twice
- Therefore, $0 < T_{dq} + T_{dl} - T_{dc} < T_C$

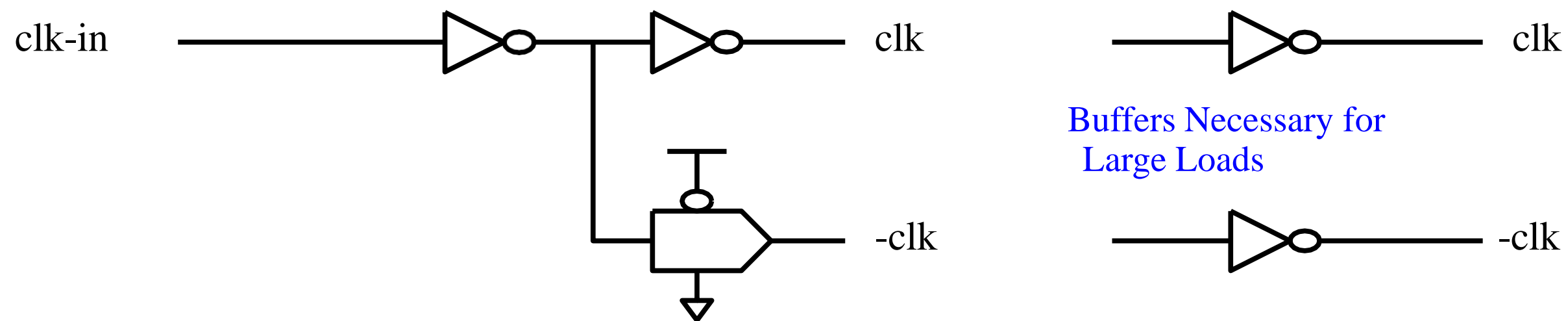
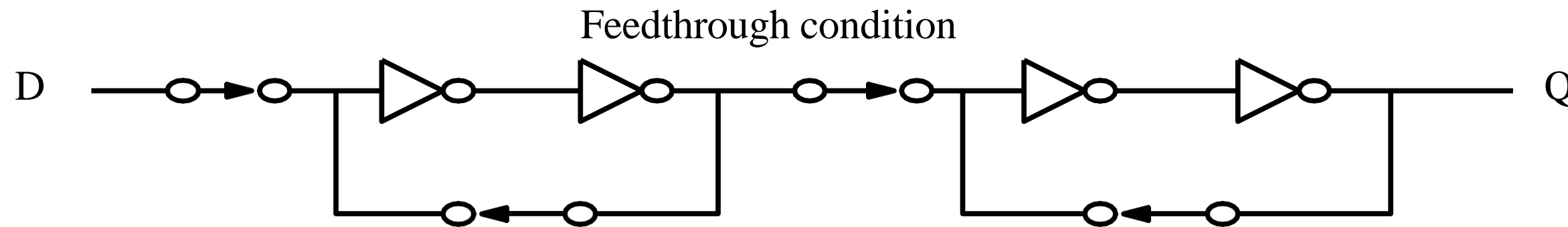
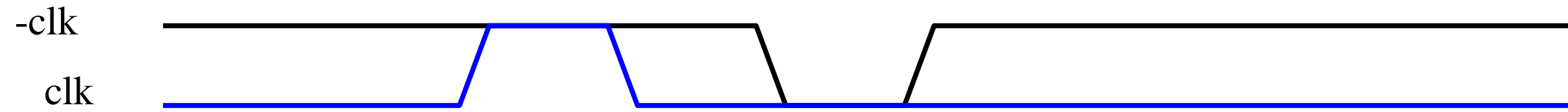


D REGISTER



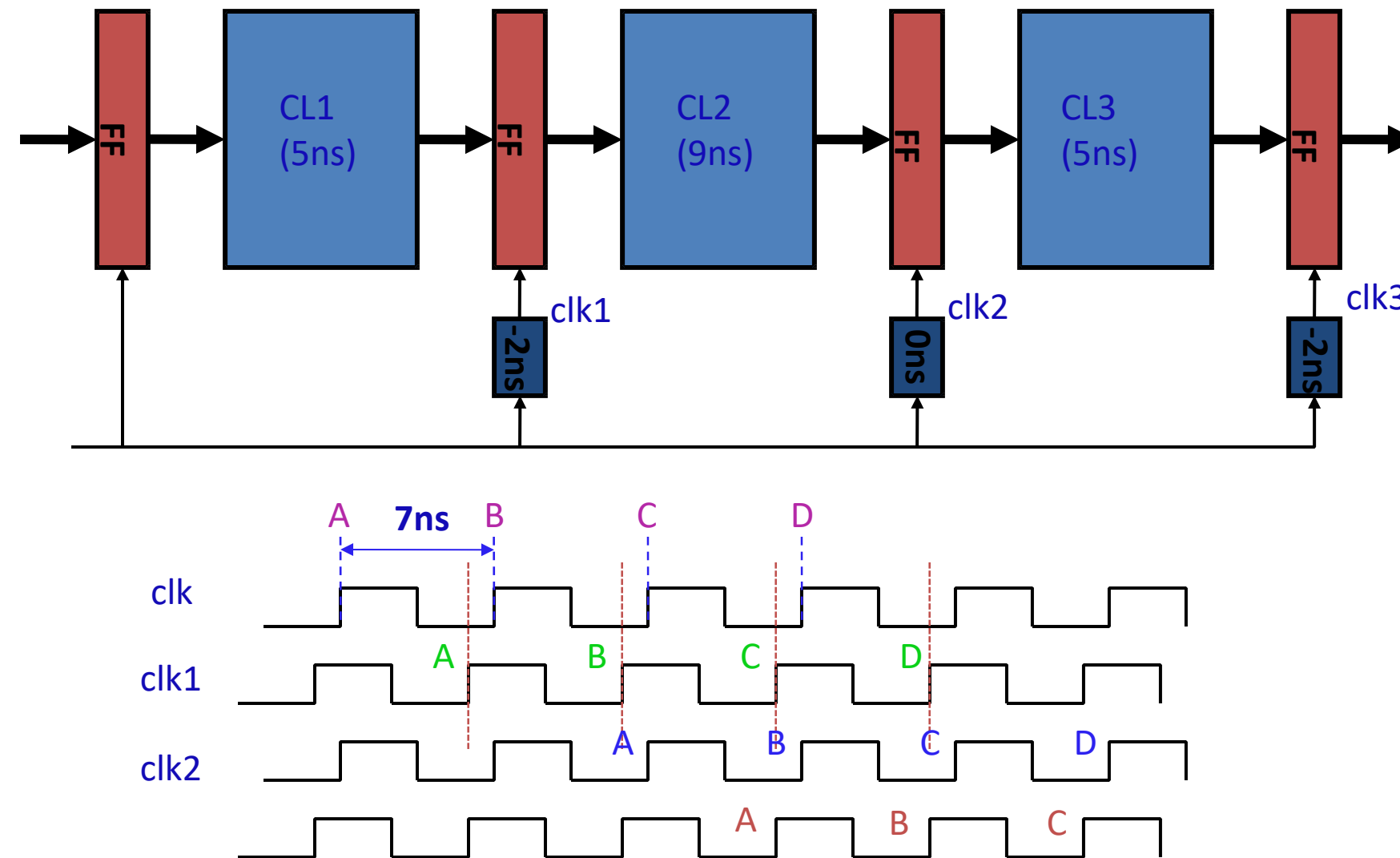


CLOCK SKEW

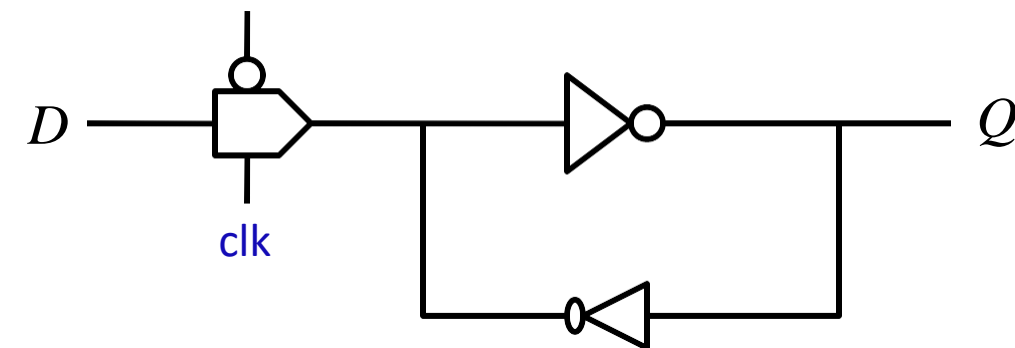




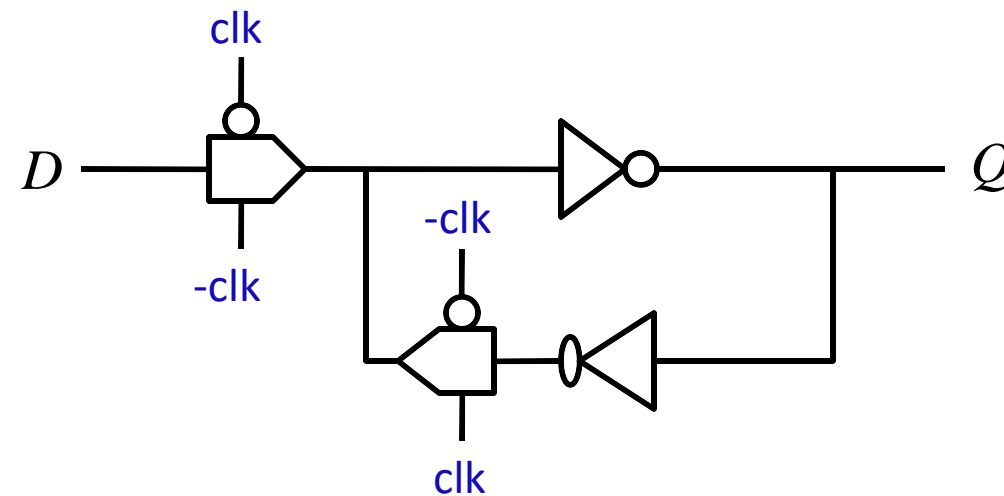
STRATEGIES—SKEW CLOCK PIPELINE



LATCHES

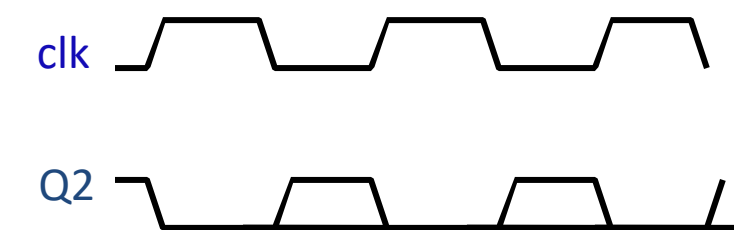
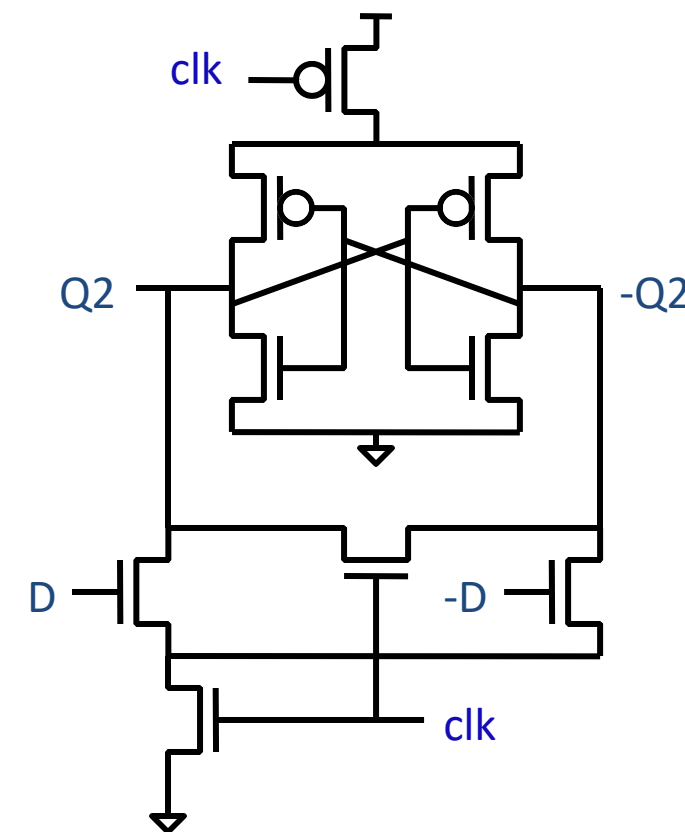
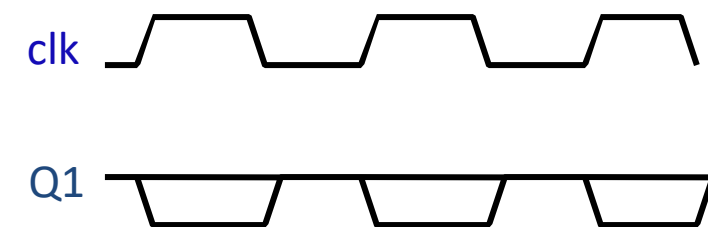
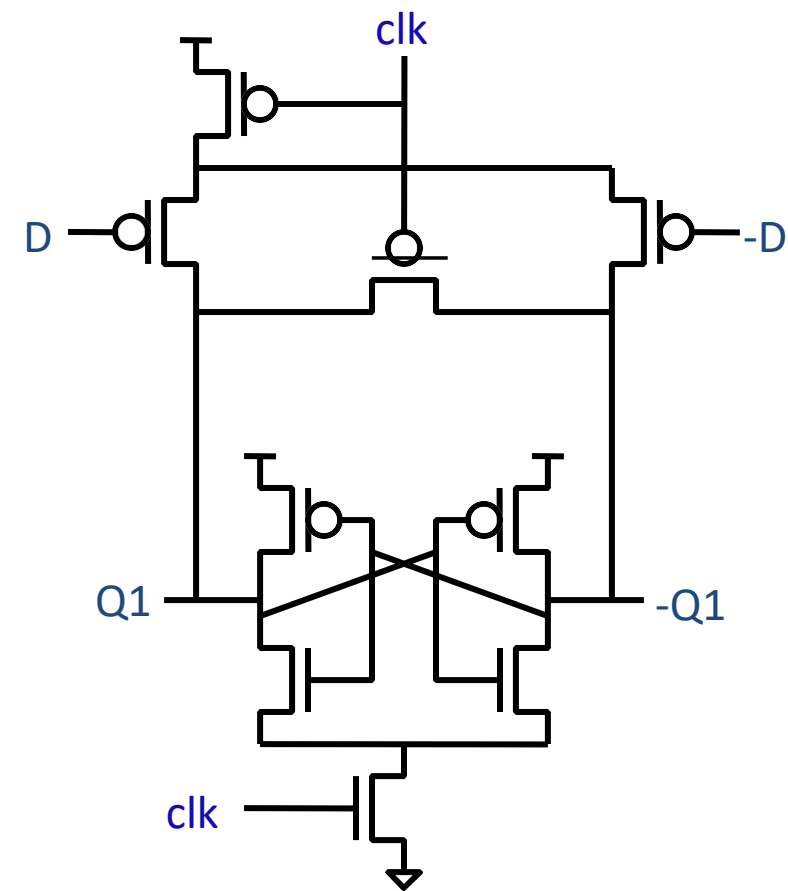


1. Low area cost
2. Driving capability of D must override the feedback inverter



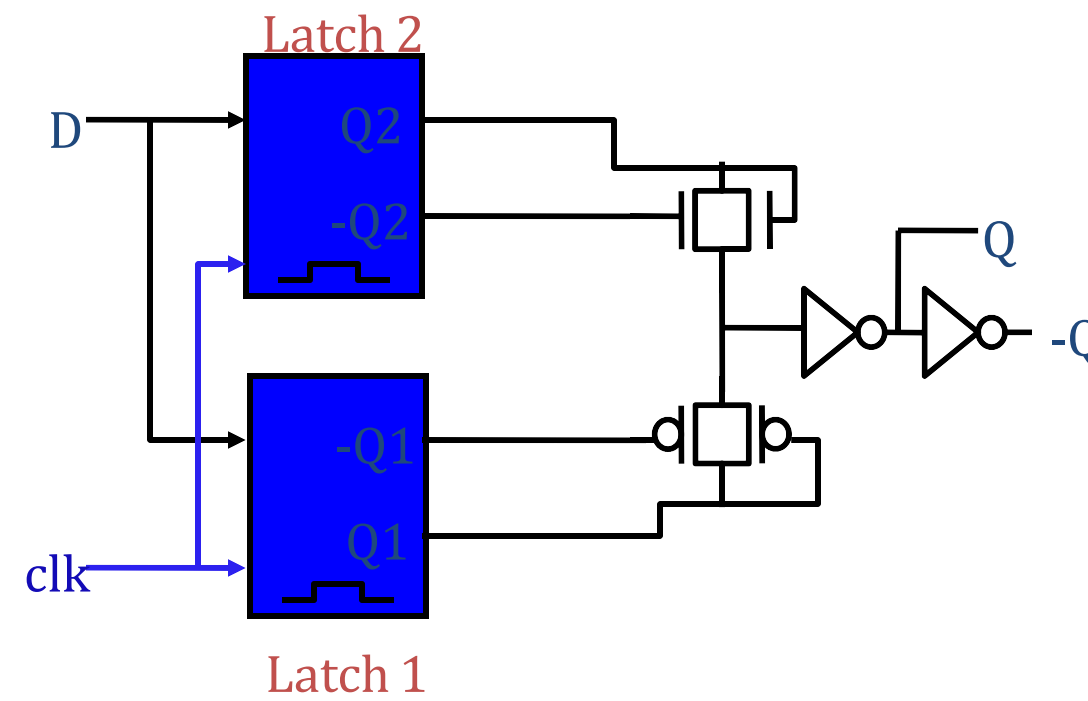


DETDFE –LATCH 1 & 2





DET DFF

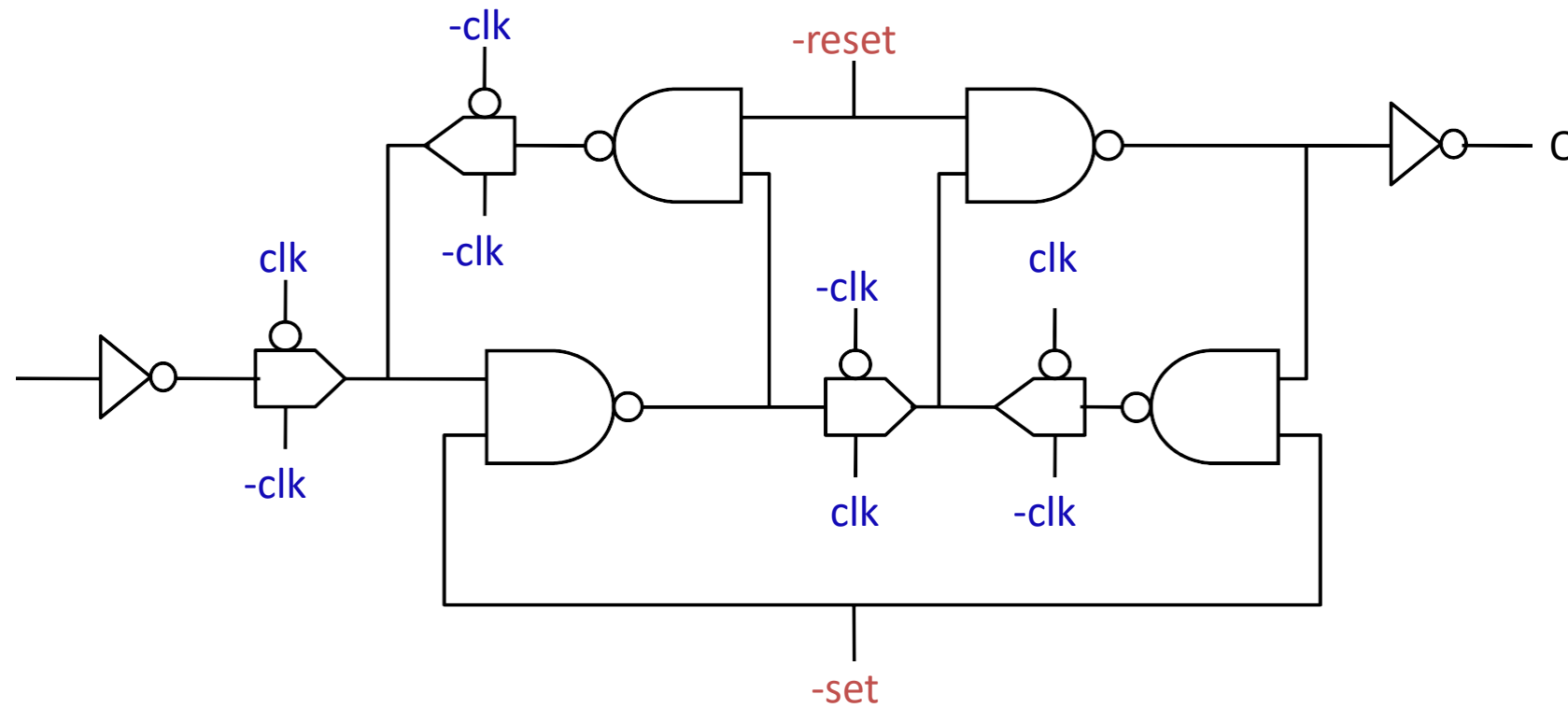


clk $\overline{\text{Latch 1 enabled}}$ $\overline{\text{Latch 2 enabled}}$
 $Q2 = -Q2 = \text{low}$ $Q1 = -Q1 = \text{high}$





ASYNCHRONOUSLY SETTABLE & RESETTABLE REGISTER

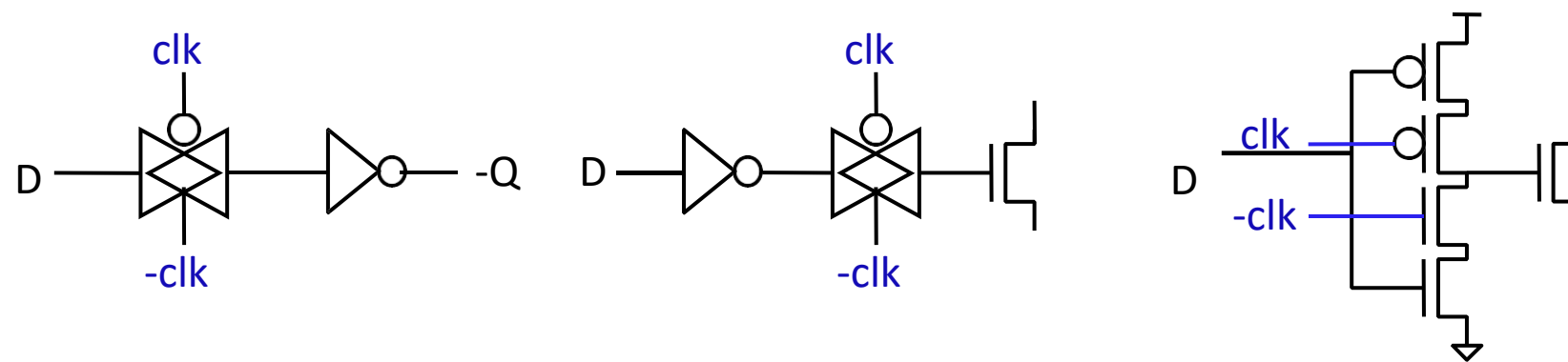




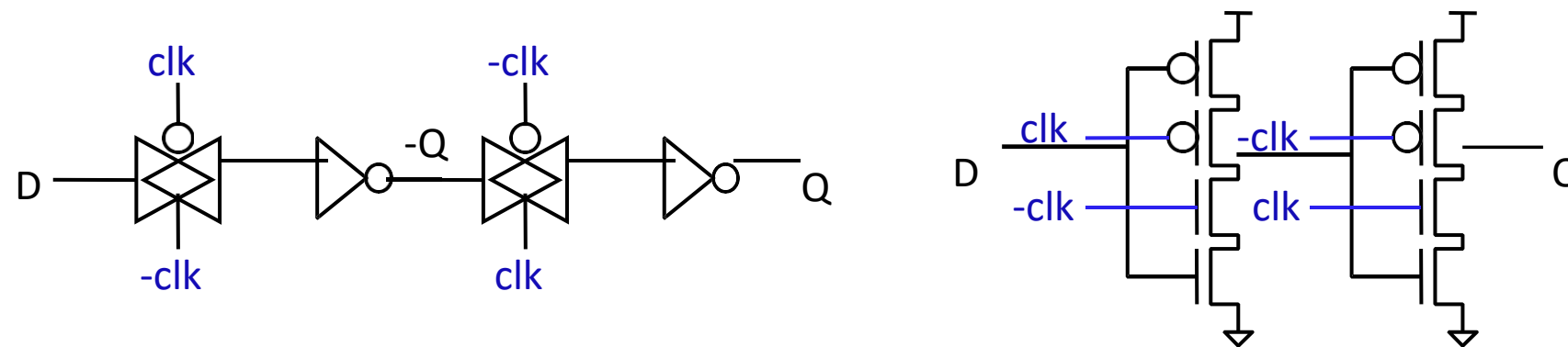
DYNAMIC REGISTERS & SINGLE CLOCK



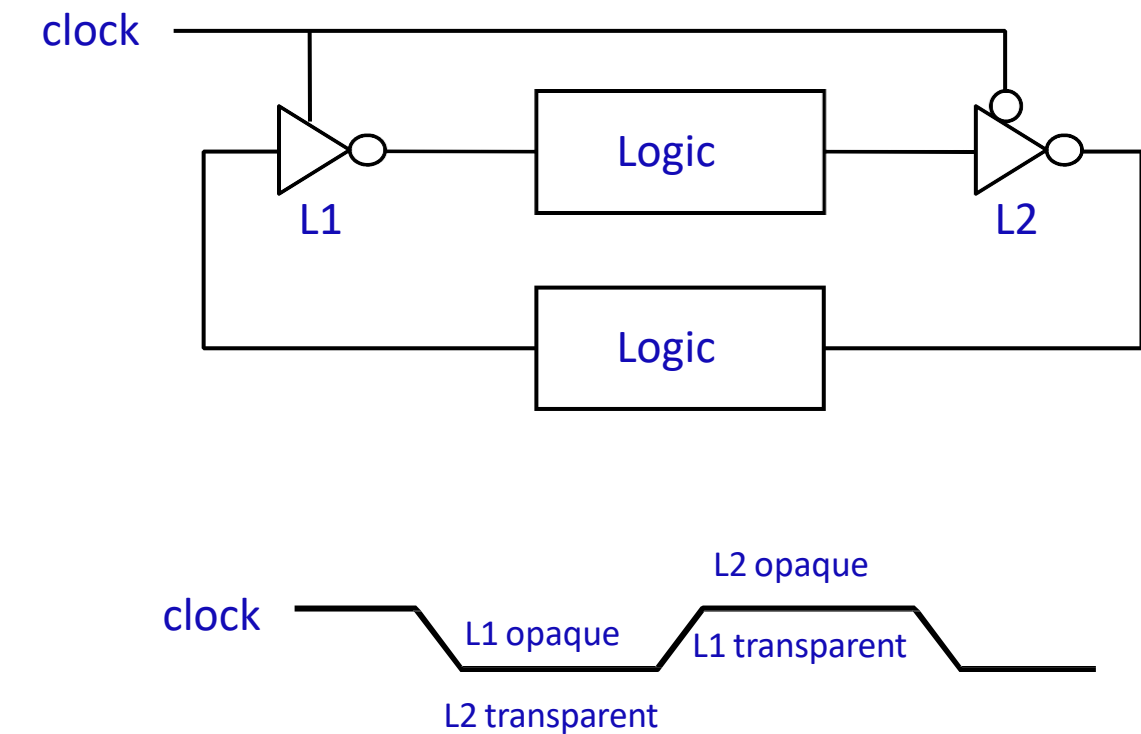
Dynamic single clock latches



Dynamic single clock registers



single clock





ASSESSMENT



1. Compare System timing-setup & hold time
2. Differentiate & Draw the clock strategies of Asynchronously settable & resettable register
3. Define Clock Skew





SUMMARY & THANK YOU