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PROCESSOR AND PIPELINE

Fundamental Concept

Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction takes place in a pipelined processor. 3 stages that a works on the concept of pipline operation inserting the bottle (I), Filling water in the bottle (F) and sealing the bottle (S).

Without pipelining = 9/3 minutes = 3m

I F S
I I I F S
I I I I F S (9 minutes)

with pipelining = 5/3 minutes = 1.67m

IFS II
IIFSI
IIIFS (5 minutes)

Design of a basic pipeline:

- In a pipelined processor a pipeline has two ends the input end and the output end. Between these the output of one stage is connected to the input of the next stage and each stage performs a specific operation
- Interface registers are used to hold the intermediate output between two stages. These interface registers are also called latch or buffer
- All the stages in the pipeline along with the interface registers are controlled by a common clock.

Execution in a pipelined process: Execution sequence of instructions in a pipelined process can be visualized using a space time diagram for example, consider a processor having 4 stages and let there be 2 instructions to be executed. we can visualize the execution sequence through the following space-time diagrams:

non-overlapping execution

stage / cycle	1	2	3	4	5	6	7	8
S1	I1				I2			
S2		I1				I2		
S3			I1				I2	
S4				I1				I2

Total time = 8 cycle

overlapped execution:

Stage / cycle	1	2	3	4	5
S1	I1	I2			
S2		I1	I2		
S3			I1	I2	
S4				I1	I2

Total time = 5 cycle

Stage 1 (Instruction fetch): In this stage the CPU reads instructions from the address in the memory, whose value is present in the program counter

Stage 2 (Instruction Decode): In this stage instruction is decoded and the register file is accessed to get the values from the registers used in the instruction.

Stage 3 (Instruction Execute): In this stage ALU operations are performed.

Stage 4 (memory Access): In this stage memory operands are read and written from/to the memory that is present in the instruction.

Stage 5 (write Back): In this stage computed/Fetched value is written back to the register present in the instruction.

Performance of a pipelined processor:

Consider a "k" segment pipeline with clock cycle time as "TP". Let there be "n" tasks to be completed in the pipelined processor. The first instruction is going to take "k" cycles. to come out of the pipeline but the other 'n-1' instructions will take only "1" cycle total of "n-1" cycles. So time taken to execute "n" instructions in a pipelined processor.

ET pipeline = K+n-1 cycles
= (K+n-1) TP

Same case for a nonpipelined processor, the execution time of 'n' instructions

ET non - pipeline = n * K * TP

Speedup (S) of the pipelined processor over the non-pipelined processor when "n" takes are executed on the same processor is

S = performance of non pipelined processo
/performance of pipelined processo

As the performance of a processor is inversely proportional to the execution time we have,

S = ET non-pipeline / ET pipeline

⇒ S = [n * K * TP] / [(K+n-1) * TP]

S = [n*K] / [K+n-1]

when the number of tasks "n" is significantly larger than K than is n >> K

S = n * K / n S = K

Efficiency = Given speed up / Max speed up

$= S / S_{max}$.

we know that $S_{max} = K$.

Efficiency $= S/K$.

Throughput = number of instructions / Total time to complete the instruction

Throughput $= n / (k+n-1) * TP_{note}$

Throughput :

- It measure number of instruction completed per unit time
- It Represents overall processing speed of pipeline.
- Higher throughput indicate processing speed of pipeline
- Calculated as throughput = number of instruction executed / execution time.
- It can be affected by pipeline length clock frequency. efficiency of instruction execution and presence of pipeline hazards or stalls.

Execution of a complete Instruction.

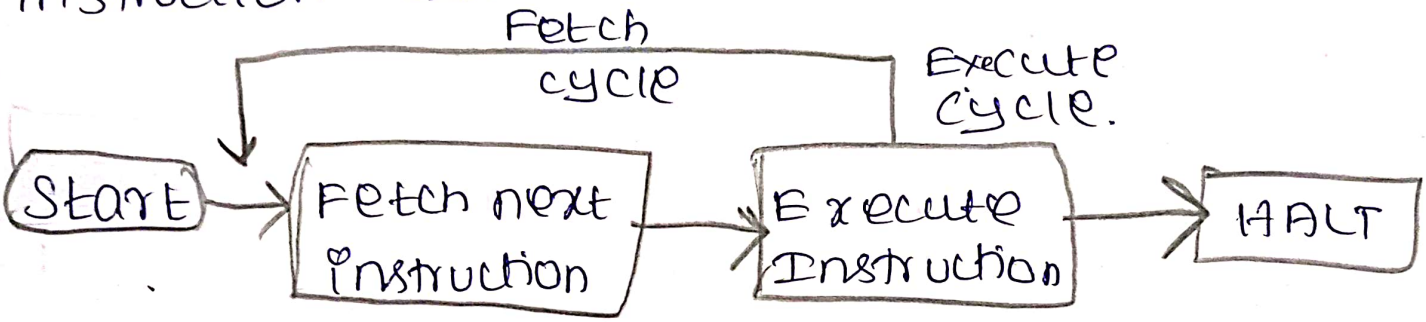
An instruction cycle consists of an instruction fetch, followed by zero or more operand fetches, Int. Followed by zero or more operand stores, Followed by an interrupt check need to be inter connected in order to exchange data and control signals.

Control Unit: A computer can be programmed by using a small set of basic logic components that store binary data and perform arithmetic and logical operations on data. If a particular computation is to be performed, a configuration of logic components designed specifically for that computation could be constructed. programming in hardware is termed a hardwired program. This customized hardware system

accept data and produces result. This customized hardware system is not very flexible because for each new program this customized hardware must be rewired. The new method of programming a sequence of codes or instructions is called software (microprogram). The CPU exchanges data with memory. The CPU typically makes use of two internal registers: a memory address register (MAR) which specifies the address in memory for the next read or write and a memory data register (MDR) which contains the data to be written into memory or receives the data read form memory.

Instruction cycle: The basic function performed by a computer is execution of a program which consists of a set of instructions stored in memory. The processor does the actual work by executing instructions specified in the program. In the simplest form, instruction processing consists of two steps: the processor reads (fetches) instruction from memory one at a time and executes

each instruction. The processing required for a single instruction is called an instruction cycle.



- The processor fetches an instruction from memory - program counter (PC) register holds the address of the instruction to be fetched next
- The processor increments the PC after each instruction fetch so that it will fetch the next instruction in the sequence - unless told otherwise.
- The fetched instruction is loaded into the instruction register (IR) in the processor the instruction contains bits that specify the action the proces will take

- The processor interprets the instruction and performs the required action In general these actions fall into four categories :-

<u>processor memory :</u> Data transferred to or From the processor to memory.

<u>processor - I/O :</u> Data transferred to or From a peripheral device by transferring between the processor and an I/O module

<u>Data processing :</u> The processor performs some arithmetic or logic operation on data

<u>Control :</u> an instruction may specify that the sequence of execution be altered an instruction execution may involve a combination of these actions.