



SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore - 641 107

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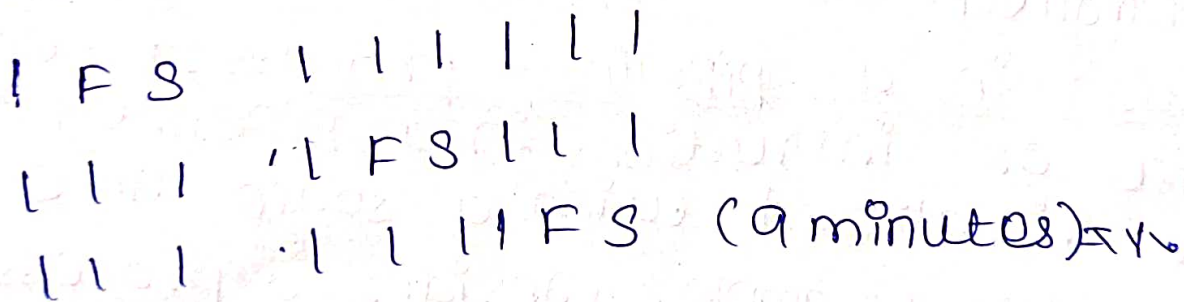


PROCESSOR AND PIPELINE

fundamental concept

Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Simultaneous execution of more than one instruction takes place in a pipelined processor. 3 stages that a works on the concept of pipeline operation inserting the bottle (1), Filling water in the bottle (2) and sealing the bottle (3).

without pipelining = $9/3$ minutes = 3m



with pipelining = $5/3$ minutes = 1.67m

IFS 11

11FS 1

11IFS (15 minutes)

Design of a basic pipeline:

- In a pipelined processor a pipeline has two ends the input end and the output end. Between these the output of one stage is connected to the input of the next stage and each stage performs a specific operation
- Interface registers are used to hold the intermediate output between two stages. These interface registers are also called latch or buffer
- All the stages in the pipeline along with the interface registers are controlled by a common clock.

Execution in a pipelined process: Execution

Sequence of instructions in a pipelined process can be visualized using a space time diagram. For example, consider a processor having 4 stages and let there be 2 instructions to be executed. We can visualize the execution sequence through the following space-time diagrams:



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non-overlapping execution

stage / cycle	1	2	3	4	5	6	7	8
S1	11				12			
S2		11				12		
S3			11				12	
S4				11				12

Total time = 8 cycle

overlapped execution:

stage / cycle	1	2	3	4	5
S1	11	12			
S2		11	12		
S3			11	12	
S4				11	12

Total time = 5 cycle

Stage 1 (Instruction fetch): In this stage the CPU reads instructions from the address in the memory, whose value is present in the program counter.

Stage 2 (Instruction Decode): In this stage instruction is decoded and the register file is accessed to get the values from the registers used in the instruction.

Stage 3 (Instruction Execute): In this stage ALU operations are performed.

Stage 4 (Memory Access): In this stage memory operands are read and written from/to the memory that is present in the instruction.

Stage 5 (Write Back): In this stage computed / fetched value is written back to the register present in the instruction.

Performance of a pipelined processor:

Consider a " k " segment pipeline with clock cycle time as " T_p ". Let there be " n " tasks to be completed in the pipelined processor. The first instruction is going to take " k " cycles to come out of the pipeline but the other ' $n-1$ ' instructions will take only ' 1 ' cycle total of ' $n-1$ ' cycles. So time taken to execute " n " instructions in a pipelined processor.



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$$\begin{aligned} \text{ET pipeline} &= k+n-1 \text{ Cycles} \\ &= (k+n-1) T_P \end{aligned}$$

Same case for a nonpipelined processor, the execution time of 'n' instructions

$$\text{ET non-pipeline} = n * k * T_P$$

Speedup (S) of the pipelined processor over the non-pipelined processor when "n" tasks are executed on the same processor is

$$S = \frac{\text{performance of non pipelined processor}}{\text{performance of pipelined processor}}$$

As the performance of a processor is inversely proportional to the execution time we have,

$$S = \frac{\text{ET non-pipeline}}{\text{ET pipeline}}$$

$$\Rightarrow S = \frac{[n * k * T_P]}{[(k+n-1) * T_P]}$$

$$S = \frac{[n * k]}{[k+n-1]}$$

when the number of tasks "n" is significantly larger than k than is $n \gg k$

$$S = n * k / n \quad S = k$$

$$\text{Efficiency} = \text{Given speed up} / \text{Max speed up}$$

$$= S / S_{\text{max}}$$

We know that $S_{\text{max}} = k$.

$$\text{Efficiency} = S / k$$

Throughput = number of instructions / Total time to complete the instruction

$$\text{Throughput} = n / (k + n - 1) \times \text{TP}_{\text{nope}}$$

Throughput:

- It measures number of instruction completed per unit time
- It represents overall processing speed of pipeline.
- Higher throughput indicate processing speed of pipeline
- calculated as $\text{throughput} = \text{number of instruction executed} / \text{execution time}$.
- It can be affected by pipeline length, clock frequency, efficiency of instruction execution and presence of pipeline hazards or stalls.