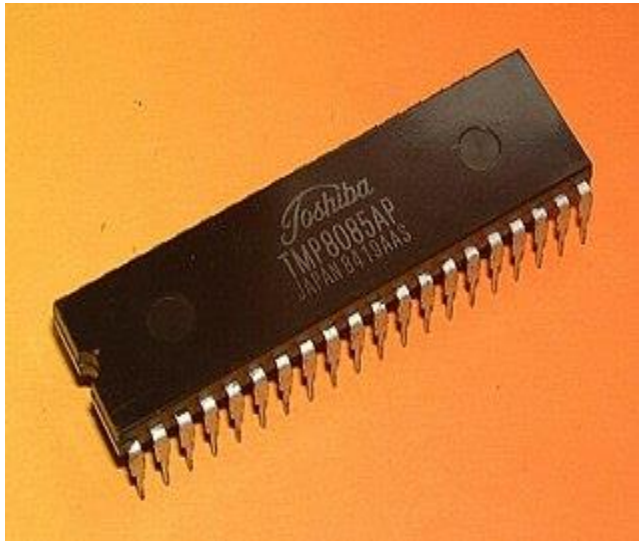
SNS COLLEGE OF ENGINEERING

(Autonomous)

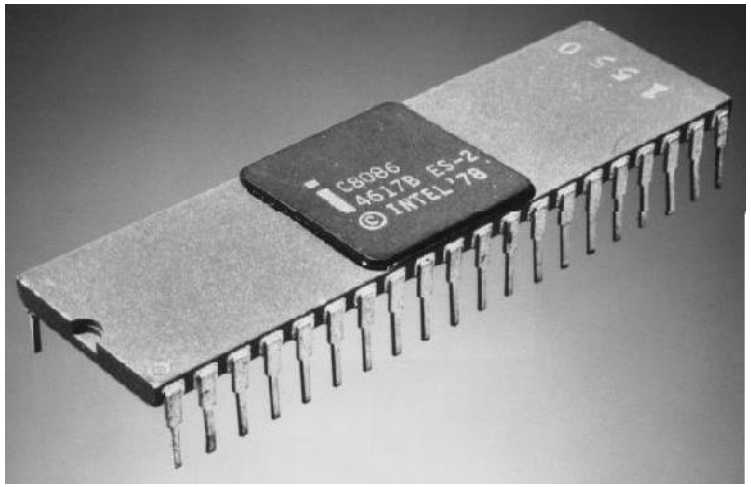
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

23ECB204 – DIGITAL ELECTRONICS AND MICROPROCESSOR



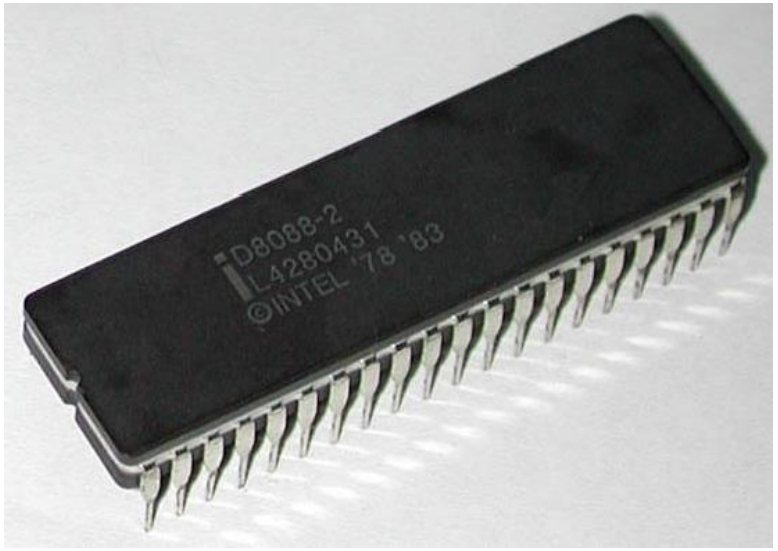
16-bit Microprocessors

INTEL 8086



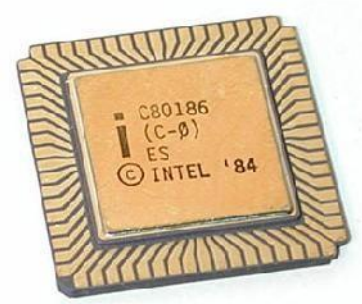
- Introduced in 1978.
- It was first 16-bit µP.
- Its clock speed is 4.77 MHz, 8 MHz and 10 MHz, depending on the version.
- Its data bus is 16-bit and address bus is 20-bit.
- It had 29,000 transistors.
- Could execute 2.5 million instructions per second.
- It could access 1 MB of memory.
- It had 22,000 instructions.
- It had ***Multiply*** and ***Divide*** instructions.

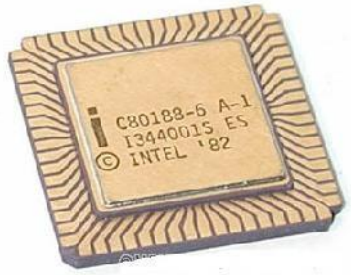
INTEL 8088



- Introduced in 1979.
- It was also 16-bit µP.
- It was created as a cheaper version of Intel's 8086.
- It was a 16-bit processor with an 8-bit external bus.

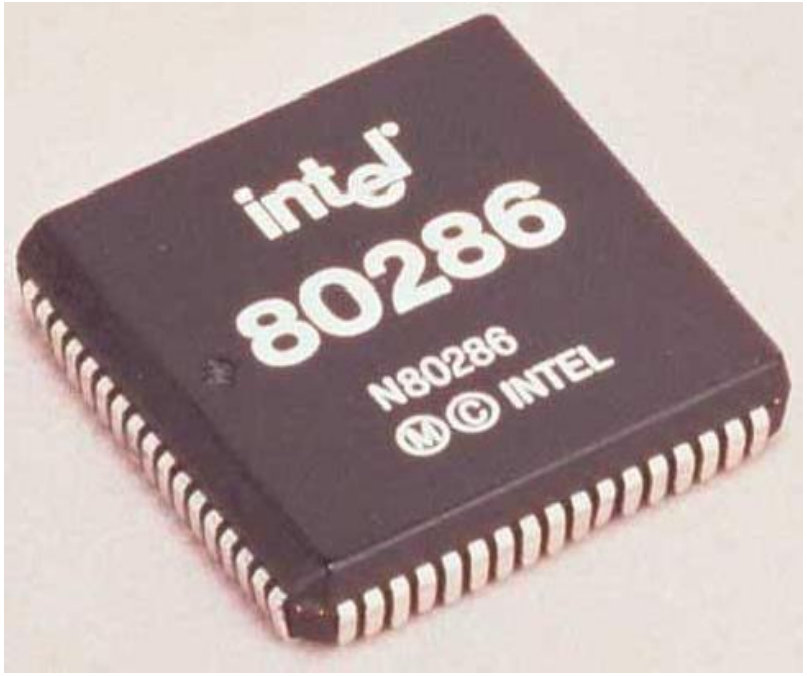
INTEL 80186 & 80188





- Introduced in 1982.
- They were 16-bit µPs.
- Clock speed was 6 MHz.
- 80188 was a cheaper version of 80186 with an 8-bit external data bus.

INTEL 80286



- Introduced in 1982.
- It was 16-bit µP.
- Its clock speed was 8 MHz.
- Its data bus is 16-bit and address bus is 24- bit.
- It could address 16 MB of memory.
- It had 1,34,000 transistors.

32-BIT MICROPROCESSORS

INTEL 80386

- Introduced in 1986.
- It was first 32-bit µP.
- Its data bus is 32-bit and address bus is 32- bit.
- It could address 4 GB of memory.
- It had 2,75,000 transistors.
- Its clock speed varied from 16 MHz to 33 MHz depending upon the various versions.

INTEL 80486

- Introduced in 1989.
- It was also 32-bit µP.
- It had 1.2 million transistors.
- Its clock speed varied from 16 MHz to 100 MHz depending upon the various versions.
- 8 KB of cache memory was introduced.

INTEL PENTIUM

- Introduced in 1993.
- It was also 32-bit µP.
- It was originally named 80586.
- Its clock speed was 66 MHz.
- Its data bus is 32-bit and address bus is 32-bit.

INTEL PENTIUM PRO

- Introduced in 1995.
- It was also 32-bit µP.
- It had 21 million transistors.
- Cache memory:
  - 8 KB for instructions.
  - 8 KB for data.

INTEL PENTIUM II

- Introduced in 1997.
- It was also 32-bit µP.
- Its clock speed was 233 MHz to 500 MHz.
- Could execute 333 million instructions per second.

INTEL PENTIUM II XEON

- Introduced in 1998.
- It was also 32-bit µP.
- It was designed for servers.
- Its clock speed was 400 MHz to 450 MHz.

INTEL PENTIUM III

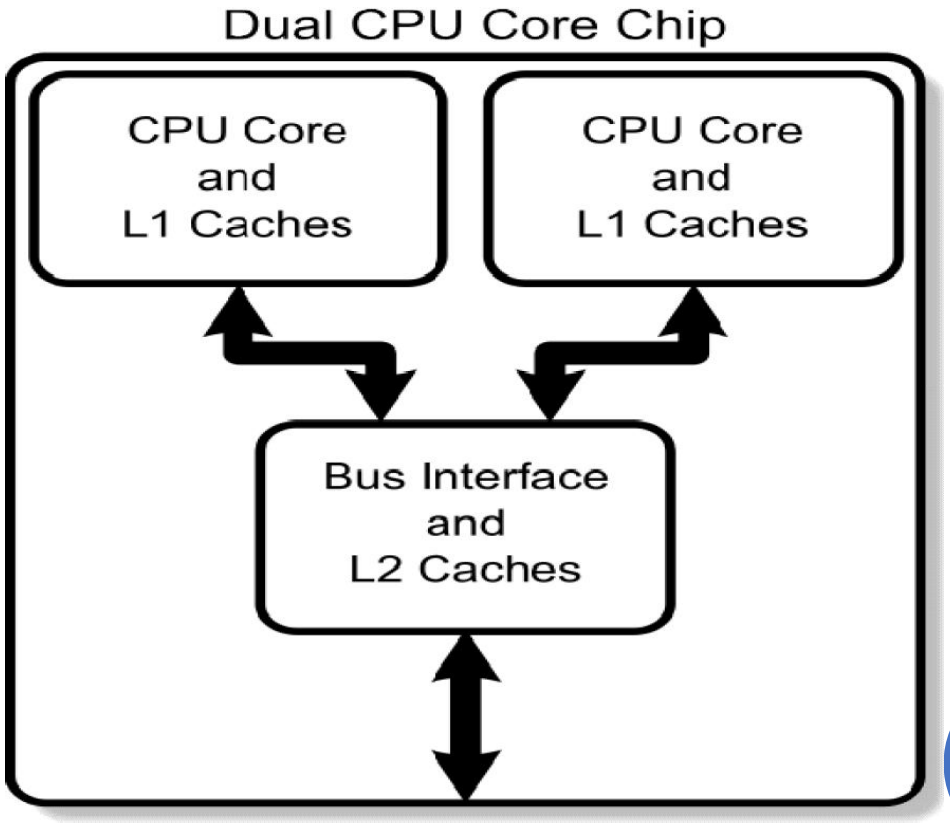
- Introduced in 1999.
- It was also 32-bit µP.
- Its clock speed varied from 500 MHz to 1.4 GHz.
- It had 9.5 million transistors.

INTEL PENTIUM IV

- Introduced in 2000.
- It was also 32-bit µP.
- Its clock speed was from 1.3 GHz to 3.8 GHz.
- It had 42 million transistors.

INTEL DUAL CORE

- Introduced in 2006.
- It is 32-bit or 64-bit µP.



64-BIT MICROPROCESSORS

Intel Core 2

Intel Core i3

INTEL CORE I5

INTEL CORE I7

BUS CONCEPT

- **BUS**: Group of conducting lines that carries data , address & control signals.

CLASSIFICATION OF BUSES:

1. **DATA BUS**: group of conducting lines that carries data.
2. **ADDRESS BUS**: group of conducting lines that carries address.
3. **CONTROL BUS**: group of conducting lines that carries control signals {RD, WR etc}

CPU BUS: group of conducting lines that directly connected to µP

SYSTEM BUS: group of conducting lines that carries data , address & control signals in a µP system

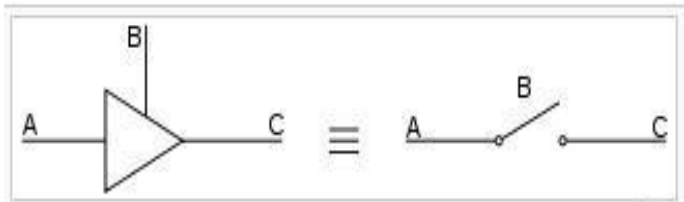
TRISTATE LOGIC

3 logic levels are:

- High State (logic 1)
- Low state (logic 0)
- High Impedance state

High Impedance: output is not being driven to any **defined** logic level by the output circuit.

INPUT		OUTPUT
A	B	C
0	1	0
1		1
X	0	Z(high impedance)



A tristate buffer can be thought of as a switch. If *B* is on, the switch is closed. If B is off, the switch is open.


Thank
you