SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ARM- Architecture

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ARE YOU USING THIS?

Introduction to ARM

- ARM, which stands for Advanced RISC Machines
- Has a significant history in the development of microprocessors.
- Especially in the mobile and embedded systems markets.

Features of ARM

- Load/store architecture
- Single-cycle execution
- Energy efficiency
- Scalability
- Customization and Licensing
- Multicore Support
- Architecture Variants
- Support for 32-bit and 64-bit Computing
- Adaptability to Various Operating Systems
- Reliability and Security

ARM Processors

- Advanced RISC Machine -

ARM Ltd. not a manufacturing Co., provides license to manufacturers

Used in high end applications involving complex computation

Hand held device, Robotic, Automation system, Consumer electronics

- Features

High performance, low power, small in size (ideal for embedded sys)

Large Register File, Small instruction set, Load-Store instructions,

Fixed length instructions, Conditional execution of instructions,

High code density, most instructions executable in single cycle,

32-bit in-line barrel shifter, built-in circuit for hardware debugging,

DSP enhanced instructions, Jazelle (Java byte code extn. 3rd state),

TrustZone (SoC approach to security)

ARM Architecture Variants

- Each family has its own instruction set, mem management, etc.

Architecture version	Processor Families	Processor	Features	Microcontroller
ARM v4T	ARM7TDMI (1995)	ARM720T ARM740T	Von Neumann, 3-stage pipeline	LPC2100 series
	ARM9TDMI	ARM920T ARM922T ARM942T	MMU, Harvard, 5-stage pipeline	SAM9G, LPC29xx, LPC3xxx, STR9
ARM v5TE, ARM v5TEJ	ARM9E (1997)	ARM926EJ-S,	MMU, DSP, Jazelle,	SAM9XE
		ARM946E-S,	MPU, DSP	
		ARM966HS	MPU (optional), DSP	
	ARM10E (1999)	ARM1020E	MMU, DSP	
		ARM1026EJ-S	MMU/MPU, DSP, Jazelle	
ARM v6	ARM11 (2003)	ARM1136J(F)-S	MMU, TrustZone, DSP, Jazelle	MSM7000, i.MX3x
		ARM1156T2(F)-S	MPU, DSP	
		ARM1176JZ(F)-S,	MMU, TrustZone, DSP, Jazelle	BCM2835

ARM Architecture Variants

Architecture version	Processor Families	Processor	Features	Microcontroller
ARM v6-M	Cortex	Cortex-M0	NVIC	LPC1200, 1100 series STM32F0x0, x1, x2
		Cortex-M1	FPGA TCM Interface, NVIC	STM32F1, F2, L1, W
ARM v7-M	Cortex	Cortex-M3	MPU (optional), NVIC	ST32F512-M, LPC1300, 1700, 1800
ARM v7-R	Cortex	Cortex-R4	MPU, DSP	STA1095, SAM4L, SAM4N, SAM4S
		Cortex-R4F	MPU, DSP, Floating Point	SAM4C, SAM4E, LPC40xx, 43xx, STM32 F3, F4
ARM v7-A	Cortex	Cortex-A8	MMU, Trust Zone, DSP, Jazelle, Neon, Floating Point	Freescale i.MX5X
		Cortex-A9	MMU, Trust Zone, Multiprocessor, DSP, Jazelle, Neon, Floating Point	Freescale i.MX6QP

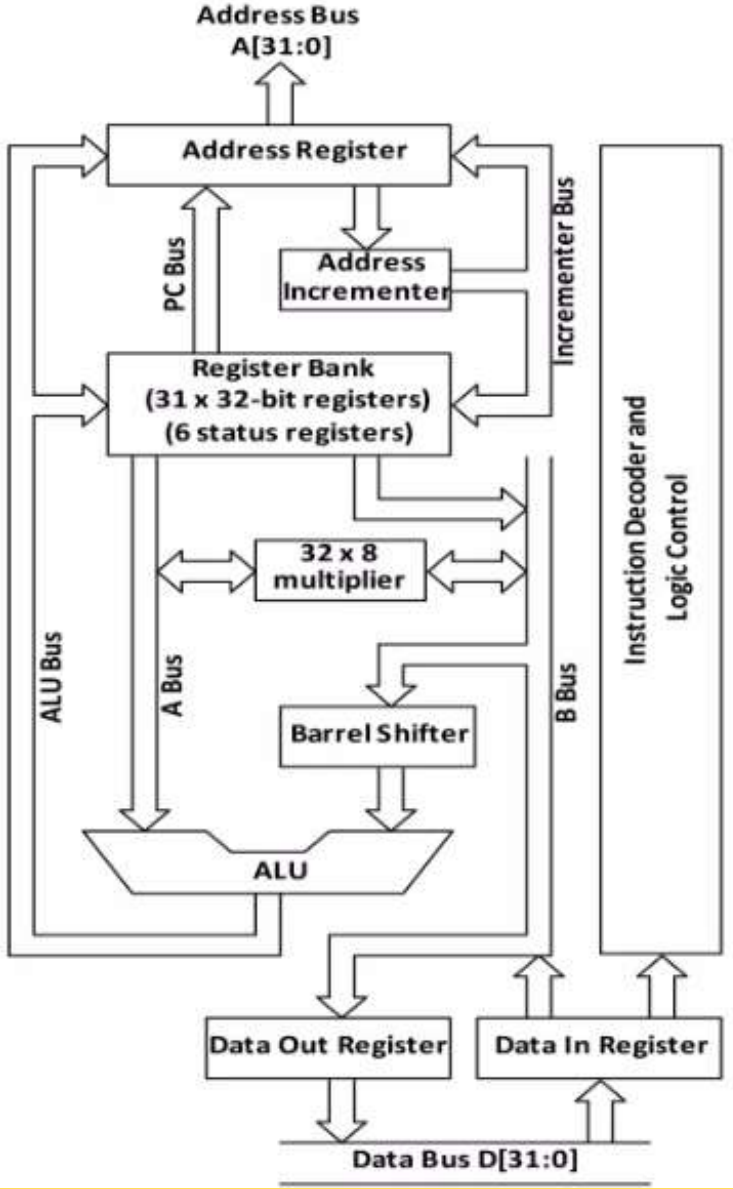
ARM Nomenclature

- A R M x y z T D M I E J F S (Example: ARM7-TDMI-S)
  - x - Series
  - y - MMU
  - z - Cache
  - T - Thumb
  - D - Debugger
  - M - Multiplier
  - I - Embedded In-Circuit Emulator (ICE) macrocell
  - E - Enhanced Instructions for DSP
  - J - JAVA acceleration by Jazelle
  - F - Floating-point
  - S - Synthesizable version

ARM7-TDMI – Internal Architecture

- Von Neumann architecture
- Data bus – 32-bit
- Address bus – 32-bit

  Addressable memory space – 4 GB
- Register bank – (31+6) 32-bit regs.
- In-line barrel shifter
- Multiplier
- ALU
- Incrementer
- Address register
- Instruction decoder & control logic



Register Organization

31 gen. purpose registers.

Only 16 regs accessible

15 registers are hidden

Named as r0 – r15

r13,r14, r15 are SP, LR, PC

8-bit/16-bit/32-bit data can be read/write

6 status registers

Only 1 is accessible

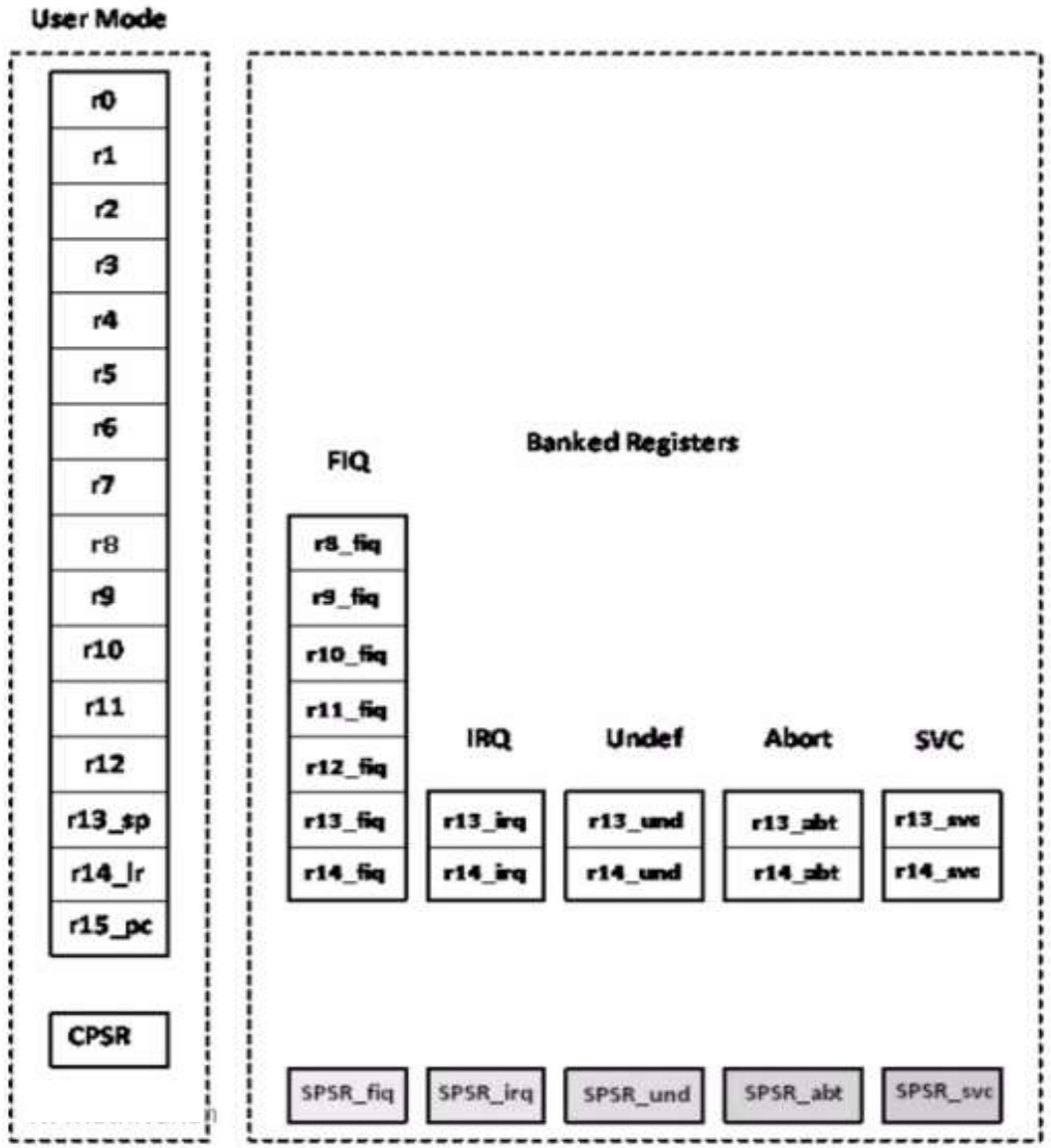
Named as CPSR, SPSR

Contains flags, control bits

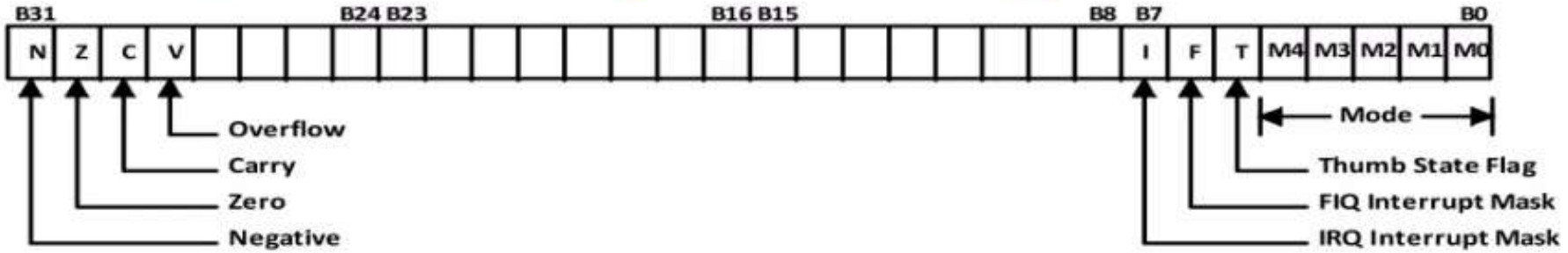
Register bank has

2 read and 1 write port and

1 read and 1 write port for PC



- Bit definitions of Program Status registers



- Barrel shifter

Combinational logic circuit

Shifts left/right any no. of bits position in one cycle

Preprocess one of data from source reg. before passed to ALU

- Multiplier

32-bit x 8-bit with early termination, Booth Algorithm

32-bit x 32-bit in 5 cycles

Non M type multiplies in 32x2-bit and for 32-bitx32-bit - 17 cycles

- **ALU**

  Connected to register bank using A-bus and B-bus

  ALU and barrel shifter operations take place in same cycle

  Result of ALU operation goes back to register bank thro' ALU bus

- **Address register**

  Holds the address of next instruction to be fetched

- **Instruction decoder and control logic**

  Enables interfacing peripherals to processors

  Has Thumb decompressor –

  Decompresses 16-bit Thumb code to 32-bit ARM code

- **Data Types**
  - Word – 32-bit, Halfword – 16-bit, Byte – 8-bit
  - Memory is byte addressable, can hold 2^{32} bytes (= 4 GB)
  - Word/ halfword /byte size data are placed at word/ halfword/ byte aligned addresses.
  - 32-bit ARM instructions are placed at word aligned addresses
- **Byte order – Endian format**
  - Word/halfword size data can be saved/retrieved in big endian or little endian format.
  - Big endian: MSB of word/halfword data are stored in lowest address and the data is addressed by address of MSB
  - Little endian: LSB of word/halfword data are stored in lowest address and the data is addressed by address of LSB

Bus Architecture

- Advanced Microcontroller Bus Architecture (AMBA)
  - Bus system connects memory, controllers and peripherals in ARM processor based microcontroller to ARM core
  - AMBA bus protocol std., adopted as on-chip bus by many μC
  - ARM core is bus master, peripherals are slaves
  - 3 buses within AMBA spec: AHP, ASP, APB
    - AHP (Advanced High-performance Bus):

      Provides high band-width.

      Supports multiple masters, slaves (e.g. of masters: DMA, Test interface, DSP, and e.g. of slaves: external memory).

      Includes bus arbiter, decoder

      Used in complex and more sophisticated systems

- **ASB (Advanced System Bus):**

  AHB and ASB have many things in common

  Both support bursting, pipelining, split transaction

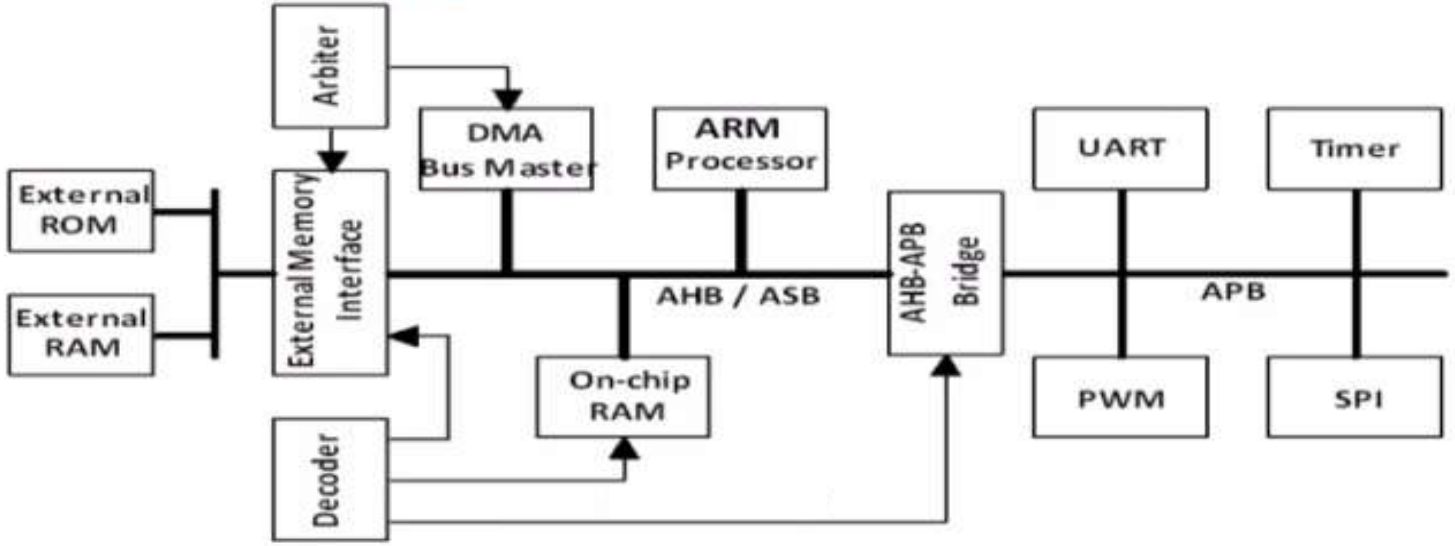
  ASB is used in simple cost effective designs

- **APB (Advanced Peripheral Bus):**

  Simple, low speed, low power bus, for UART, ... peripherals

  Implemented with simple tri-stated data bus

  AHB-APB bridge: buffers data & operations between the two



Review Questions

1. What is the size of address and data busses in ARM7 processor?
2. What is the size of memory space ARM7 processor can address?
3. List the features of ARM processors.
4. What does 'TDMI-S' in ARM7-TDMI-S refer to?
5. What are the special functions of r13, r14 and r15 registers?
6. What are special features of multiplier block in ARM7 processor?
7. What are CPSR and SPSR?
8. What are the functions of control bits of program status register?
9. What is the purpose and feature of barrel shifter?
10. Describe the internal architecture of ARM7 processor
11. List modes of operation of ARM7 processor.
12. What is the width of half-word size data?

13. Show schematically how the following data are saved in memory starting from memory address 0x0000 0000 in big endian and little endian byte order.

    Data: 0xEF, 0x1234, 0xAB, 0x6789ABCD.

14. Illustrate ARM7 processor 3-stage pipelining.
15. What is interrupt latency?
16. Illustrate braking and stalling of pipeline by branch and Load/Store instructions with suitable examples.
17. List ARM modes and the events that cause the processor to enter into the corresponding mode.
18. Which one of the ARM modes is non-privileged mode?
19. How are the privileged and non-privileged modes distinguished?
20. What are the seven types of exceptions? List the events that generate the exceptions.

ASSESSMENT

1) What is the function of Barrel Shifter?

2)What is a the size of address and data buses in ARM7 Processor?


Thank
you