SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ARM-Registers

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ARE YOU USING THIS?

ARM- The Registers

- ARM has 37 registers all of which are 32-bits long.
  - 1 dedicated program counter
  - 1 dedicated current program status register
  - 5 dedicated saved program status registers
  - 30 general purpose registers

- The current processor mode governs which of several banks is accessible. Each mode can access
  - a particular set of r0-r12 registers
  - a particular r13 (the stack pointer, sp) and r14 (the link register, lr)
  - the program counter, r15(pc)
  - the current program status register, **cpsr**

  Privileged modes (except System) can also access
  - a particular **spsr** (saved program status register)

REGISTERS

- ARM processors have 37 registers.
- The registers are arranged in partially overlapping banks.
- There is a different register bank for each processor mode.
- The banked registers give rapid context switching for dealing with processor exceptions and privileged operations.

REGISTERS

- Thirty general-purpose registers (32 bit each)
- The Program Counter (PC)
- The Application Program Status Register (APSR)
- Saved Program Status Registers (SPSRs).
- Current Program Status Registers (CPSRs).

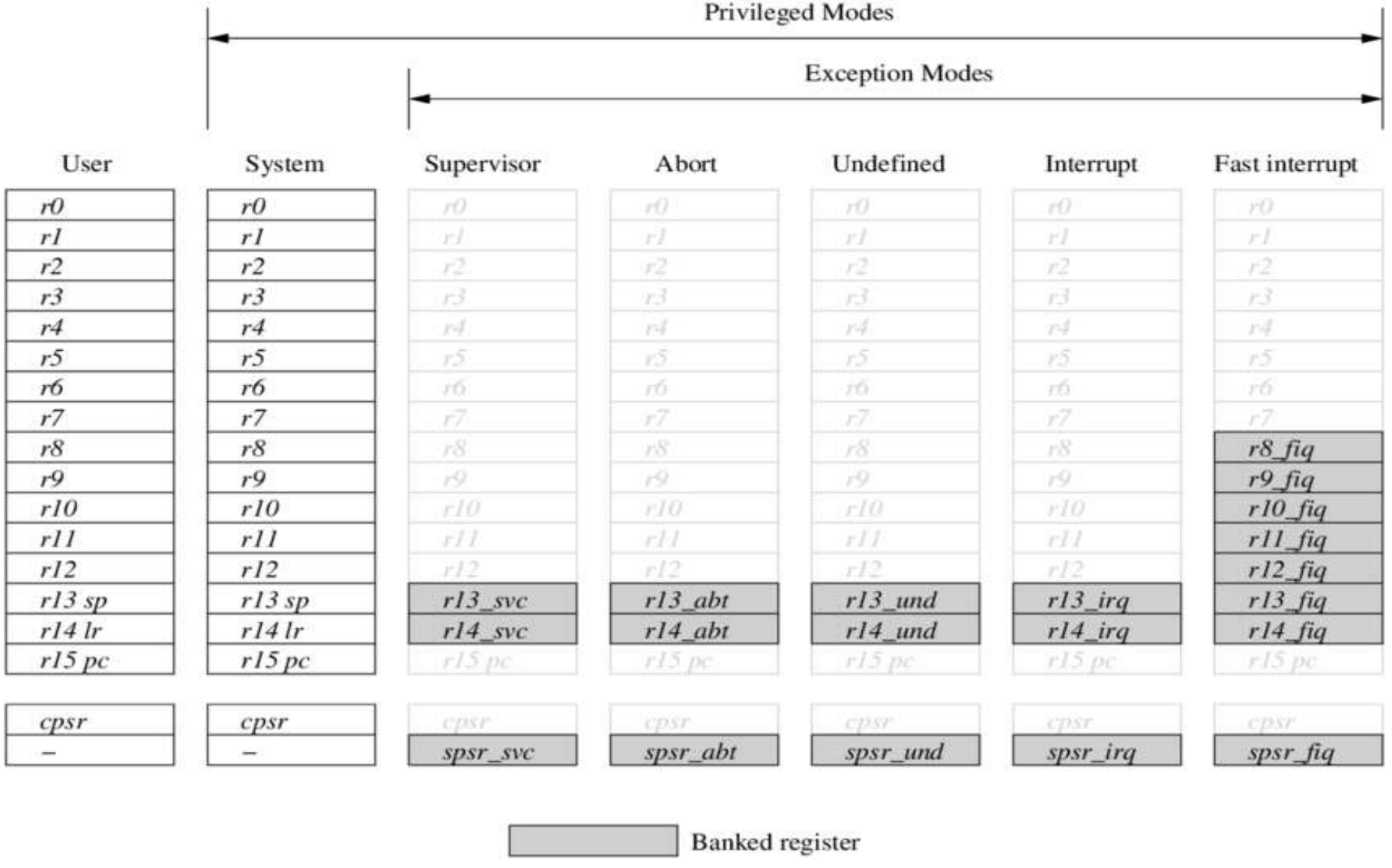
ARM- Processor Modes

- Seven basic operating modes exist:
  1. User: Unprivileged mode under which most tasks run
  2. FIQ: Entered when a high priority interrupt is raised
  3. IRQ: Entered when a low priority interrupt is raised
  4. Supervisor: Entered on reset and when a software Interrupt instruction is executed
  5. Abort: Used to handle memory access violations
  6. Undef: Used to handle undefined instructions
  7. System: Privileged mode using the same registers as user mode.

EXECUTION MODES

- A **privileged execution** has access to all resources.
- **Unprivileged execution** limits or excludes access to some resources.

REGISTERS


Privileged Modes
Exception Modes
User
System
Supervisor
Abort
Undefined
Interrupt
Fast interrupt
r0
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13 sp
r14 lr
r15 pc
cpsr
–
r13_svc
r14_svc
spsr_svc
r13_abt
r14_abt
spsr_abt
r13_und
r14_und
spsr_und
r13_irq
r14_irq
spsr_irq
r8_fiq
r9_fiq
r10_fiq
r11_fiq
r12_fiq
r13_fiq
r14_fiq
spsr_fiq
Banked register

LINK REGISTER

- r14 or lr – In user mode, used as a link register to store the return address when a subroutine call is made.

- r14 or lr – In exception mode, lr holds the return address for the exception, or a subroutine return address if subroutine calls are executed within an exception.

PROGRAM COUNTERS

- Program Counter is accessed as pc (or r15).

- It is incremented by one word (four bytes) for each instruction.
-
- Branch instructions load the destination address into pc.

Application Program Status Register (APSR)

- APSR holds copies of the Arithmetic Logic Unit (ALU) status flags.

- They are used to determine whether conditional instructions are executed or not.

Saved Program Status Registers (SPSRs)

- The SPSRs are used to store the CPSR when an exception is taken.
- User mode and System mode do not have an SPSR because they are not exception handling modes.

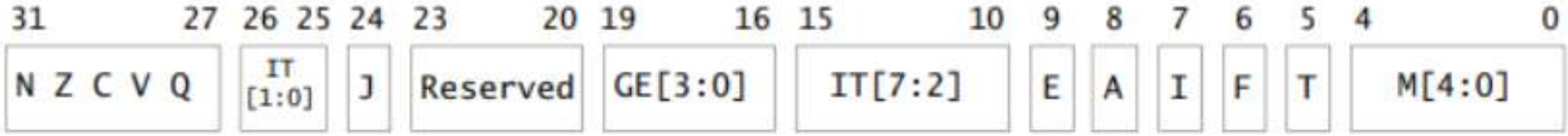
Current Program Status Register (CPSR)

The CPSR holds:

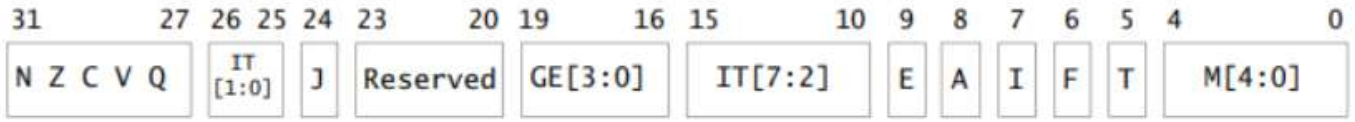
- The APSR flags
- The current processor mode
- Interrupt disable flags
- Current processor state (ARM, Thumb, or Jazelle)

Current Program Status Register (CPSR)

- CPSR to monitor and control internal operations.
- The CPSR is a dedicated 32-bit register and resides in the register file.



Current Program Status Register (CPSR)



- • N – Negative result from ALU.
- • Z – Zero result from ALU.
- • C – ALU operation Carry out.
- • V – ALU operation oVerflowed.
- • Q – cumulative saturation (also described as sticky).
- • J – indicates whether the core is in Jazelle state.
- • GE – used by some SIMD instructions.
- • IT [7:2] – If-Then conditional execution of Thumb-2 instruction groups.
- • E bit controls load/store endianness.
- • A bit disables asynchronous aborts.
- • I bit disables IRQ.
- • F bit disables FIQ.
- • T bit – indicates whether the core is in Thumb state.
- • M[4:0] – specifies the processor mode

Program Counter (r15)

- When the processor is executing in ARM state:
  - All instructions are 32 bits wide
  - All instructions must be word aligned
  - Therefore the PC value is stored in bits [31:2] with bits [1:0] undefined (as instruction cannot be halfword or byte aligned).

- When the processor is executing in Thumb state:
  - All instructions are 16 bits wide
  - All instructions must be halfword aligned
  - Therefore the PC value is stored in bits [31:1] with bit [0] undefined (as instruction cannot be byte aligned).

- When the processor is executing in Jazelle state:
  - All instructions are 8 bits wide
  - Processor performs a word access to read 4 instructions at once

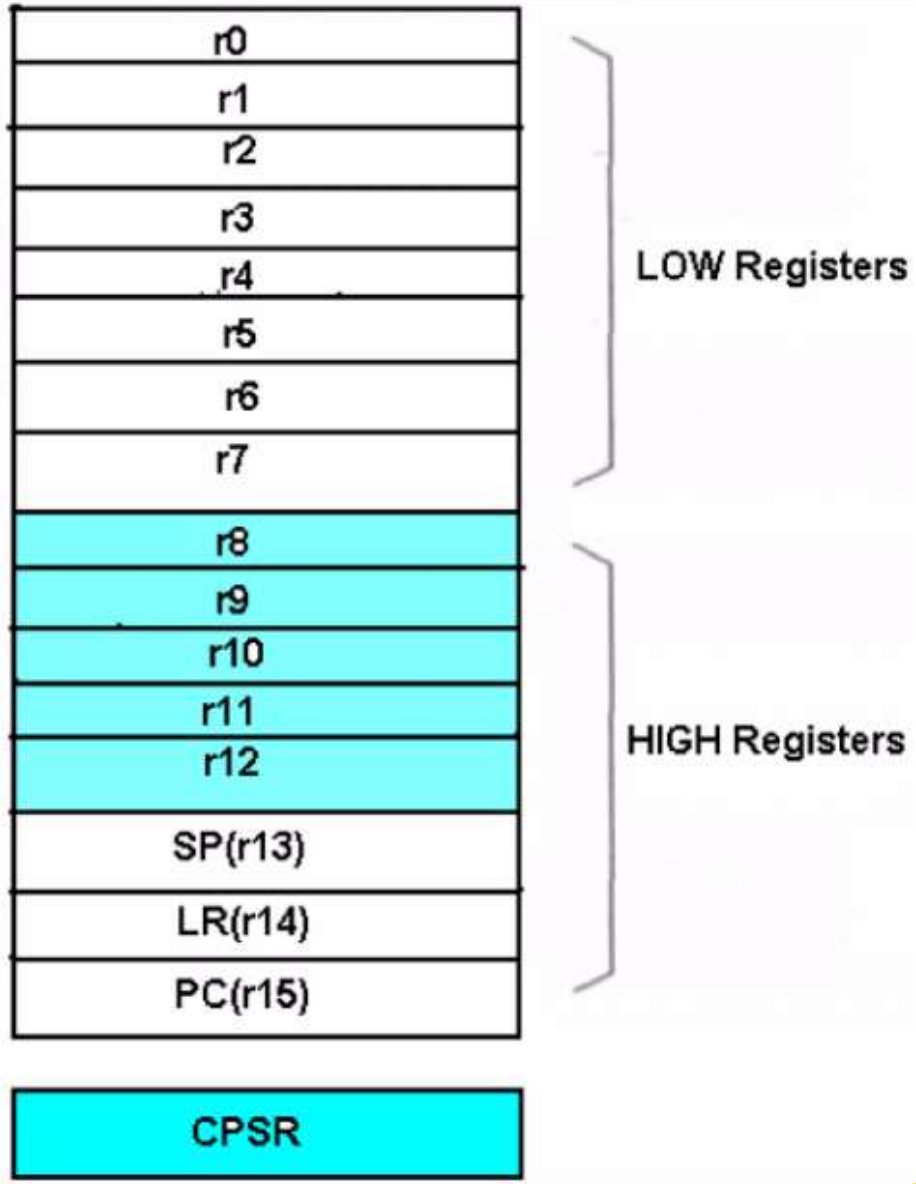
- The general purpose register usage is given below.

Ex : MOV r5, r2

ADD r1, r2

LDR r0, [r1]

STR R5,[R0]



ASSESSMENT

1) How many modes of operation is available in ARM7?

2)How many registers are available in ARM7?


Thank
you