SNS COLLEGE OF ENGINEERING

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19EC505–VLSI DESIGN

III YEAR/ V SEMESTER

SCT

UNIT 4 –VLSI TESTING

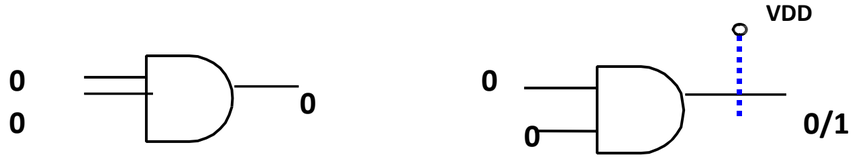
TOPIC 1 & 2–VLSI TESTING -NEEDS FOR TESTING

OUTLINE

- INTRODUCTION
- BASIC CONCEPT OF TESTING
- PRINCIPLE OF TESTING
- DIFFICULTIES IN TESTING
- HOW TO DO TESTING
- CIRCUIT MODELING
- AUTOMATIC TEST PATTERN GENERATION (ATPG)
- DIFFICULTIES IN TEST GENERATION-2 TYPES
- TESTABLE DESIGN
- ACTIVITY
- TESTING METHODS
- NEEDS OF TESTING
- DESIGN VERIFICATION
- YIELD AND REJECT RATE
- ELECTRONIC SYSTEM MANUFACTURING
- ELECTRONIC SYSTEM MANUFACTURING
- TESTING AND QUALITY
- ASSESSMENT
- SUMMARY & THANK YOU

BASIC CONCEPT OF TESTING

Testing: To tell whether a circuit is good or bad



Related fields

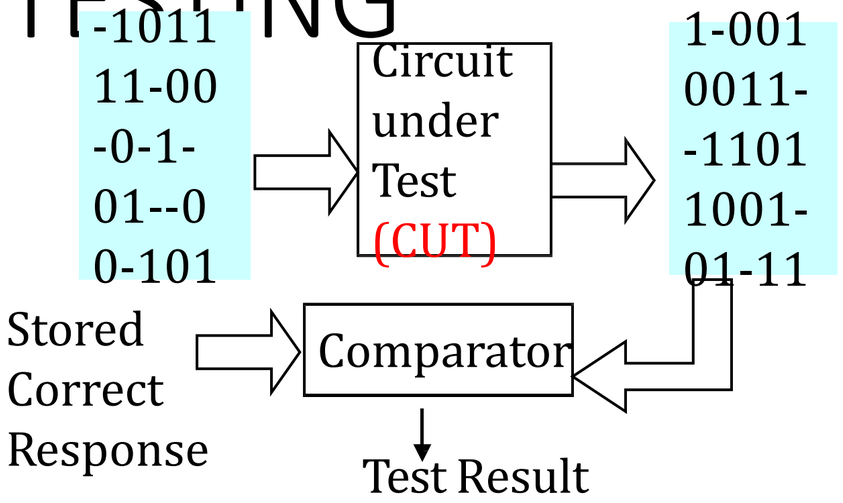
Verification: To verify the correctness of a design

Diagnosis: To tell the faulty site

Reliability: To tell whether a good system will work correctly or not after some time.

Debug: To find the faulty site and try to eliminate the fault

PRINCIPLE OF TESTING

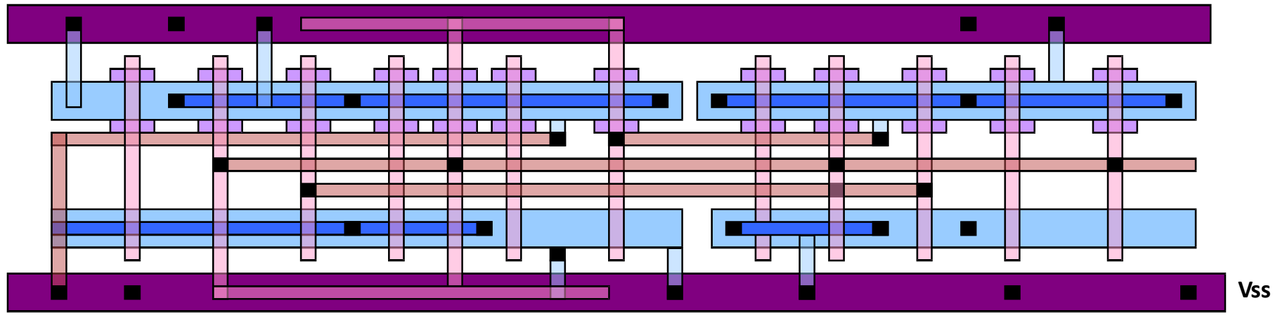


- Testing typically consists of
  - Applying set of test stimuli (input patterns, test vectors) to inputs of circuit under test (CUT), and
  - Analyzing output responses
- The quality of the tested circuits will depend upon the thoroughness of the test vectors

DIFFICULTIES IN TESTING

- Fault may occur anytime
  - Design
  - Process
  - Package
  - Field

- Fault may occur at any place



- **VLSI circuit are large**
  - Most problems encountered in testing are NP-complete
- **I/O access is limited**

HOW TO DO TESTING

From designer's point of view:

- Circuit modeling
- Fault modeling

} Modeling

- Logic simulation
- Fault simulation
- Test generation

} ATPG

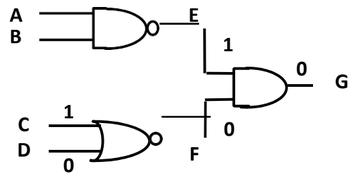
- Design for test
- Built-in self test

} Testable design

- Synthesis for testability

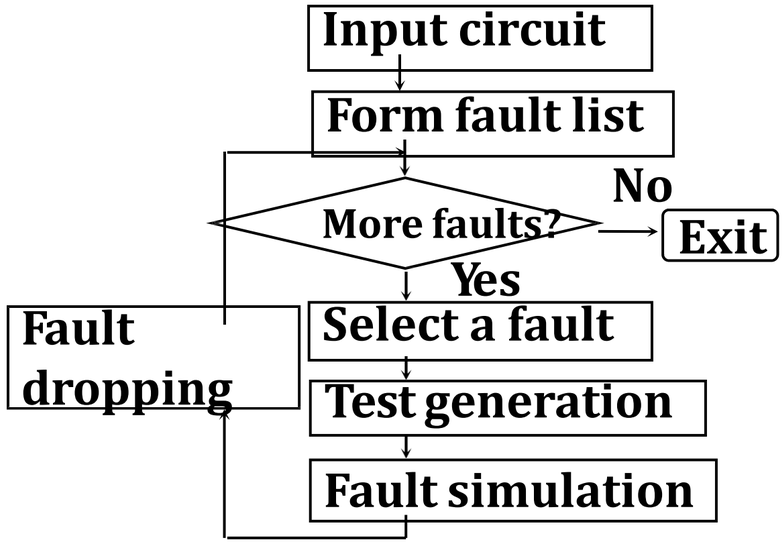
CIRCUIT MODELING

- **Functional model---** logic function
  - **f(x1,x2,...)=...**
  - **Truth table**
- **Behavioral model--- functional + timing**
  - **f(x1,x2,...)=... , Delay = 10**
- **Structural model--- collection of interconnected components or elements**



AUTOMATIC TEST PATTERN GENERATION

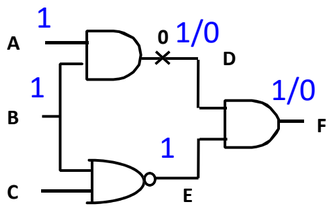
Ÿ ATPG: Given a circuit, identify a set of test vectors to detect all faults under consideration.



TEST GENERATION

- Given a fault, identify a test to detect this fault

Example:



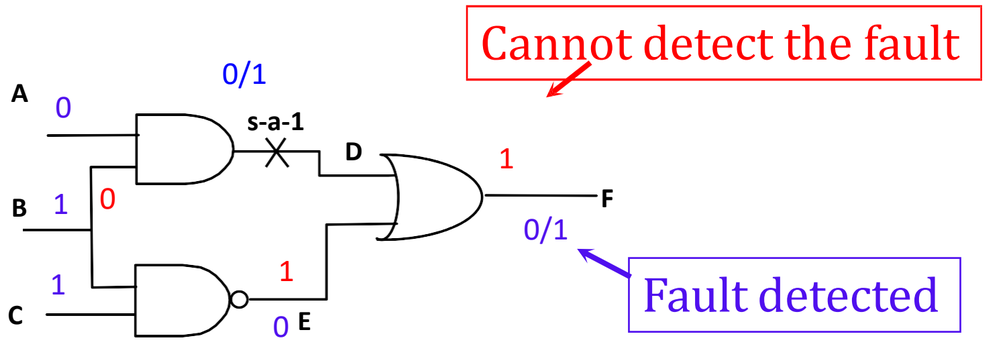
To detect D s-a-0, D must be set to 1.
Thus A=B=1.

To propagate fault effect to the primary output
E must be 1. Thus C must be 0.

Test vector: A=1, B=1, C=0

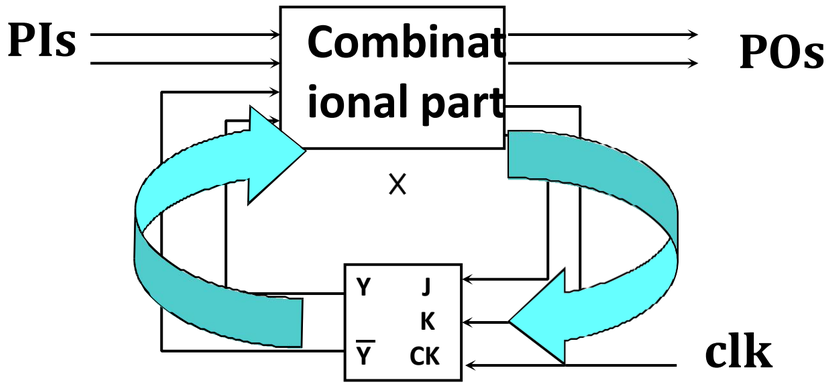
DIFFICULTIES IN TEST GENERATION

1. Reconvergent fan-out



DIFFICULTIES IN TEST GENERATION (CONT.)

2. Sequential test generation



TESTABLE DESIGN

- Design for testability (DFT)
  - ad hoc techniques
  - Scan design
  - Boundary Scan
- Built-In Self Test (BIST)
  - Random number generator (RNG)
  - Signature Analyzer (SA)
- Synthesis for Testability

CLASS ROOM ACTIVITY

Tell about yourself-any four students

To analyze how confident you are and how you present yourself.

The best way to answer this common interview question is to tell the hiring manager about your education and family background.

However, this should not look like your life's story and you should quickly concentrate on sharing a bit about your strengths that build the platform for further discussion about your suitability for the job opening.

Bonus Tips:

Don't narrate what is already mentioned in your CV

Focus more on talking about your achievements and learning

Keep it short

TESTING METHODS

- A 32-bit adder --- ATPG
- A 32-bit counter --- Design for testability + ATPG
- A 32MB Cache memory --- BIST
- A 10^7-transistor CPU --- All test techniques
- An SOC

NEEDS OF TESTING

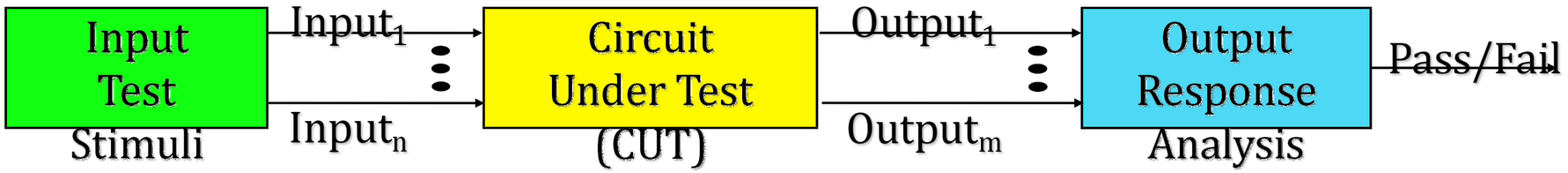
- Moore's Law results from decreasing feature size (dimensions)
  - from 10s of μm to 10s of nm for transistors and interconnecting wires
- Operating frequencies have increased from 100KHz to several GHz
- Decreasing feature size increases probability of defects during manufacturing process
  - A single faulty transistor or wire results in faulty IC
  - Testing required to guarantee fault-free products

NEEDS OF TESTING

- ***Rule of Ten*:** cost to detect faulty IC increases by an order of magnitude as we move from:
  - device → PCB → system → field operation
    - Testing performed at all of these levels
- Testing also used during
  - Manufacturing to improve yield
    - Failure mode analysis (FMA)
  - Field operation to ensure fault-free system operation
    - Initiate repairs when faults are detected

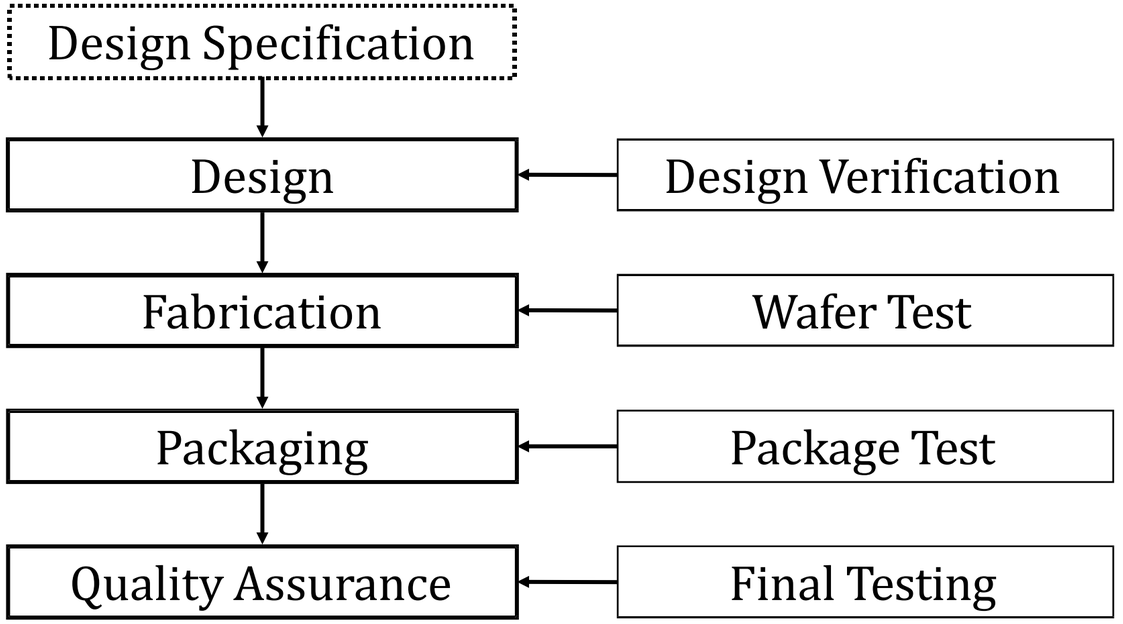
NEEDS OF TESTING

- Testing typically consists of
  - Applying set of test stimuli to
  - Inputs of ***circuit under test*** **(CUT),** and
  - Analyzing output responses
    - If incorrect (fail), CUT assumed to be faulty
    - If correct (pass), CUT assumed to be fault-free



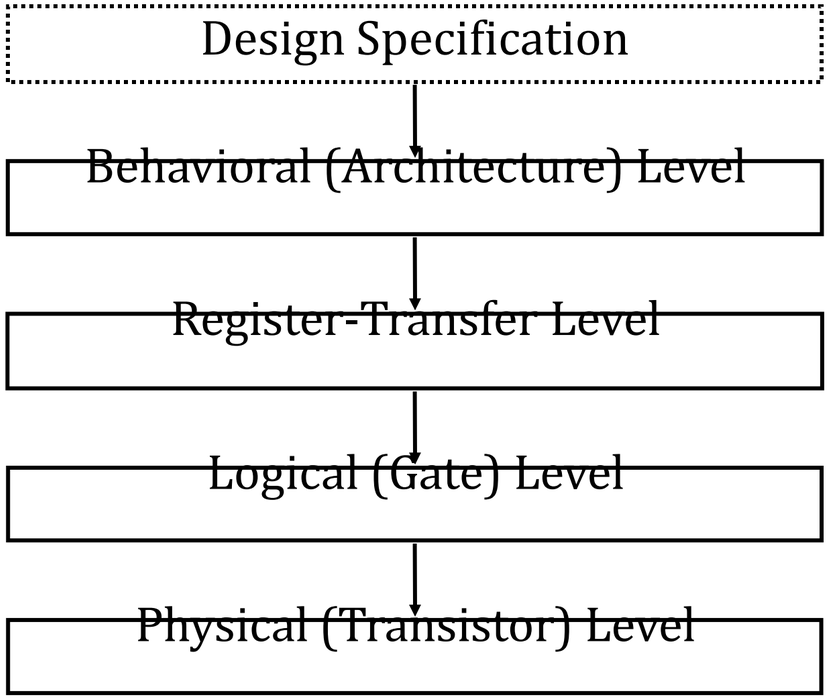
NEEDS OF TESTING

- Design verification targets design errors
  - Corrections made prior to fabrication
- Remaining tests target manufacturing defects
  - A defect is a flaw or physical imperfection that can lead to a fault



DESIGN VERIFICATION

- Different levels of abstraction during design
  - CAD tools used to synthesize design from RTL to physical level
- Simulation used at various level to test for
  - Design errors in behavioral or RTL
  - Design meeting system timing requirements after synthesis



YIELD AND REJECT RATE

- We expect faulty chips due to manufacturing defects
- 2 types of yield loss
  - Called yield

$$yield = \frac{number\ of\ acceptable\ parts}{total\ number\ of\ parts\ fabricated}$$

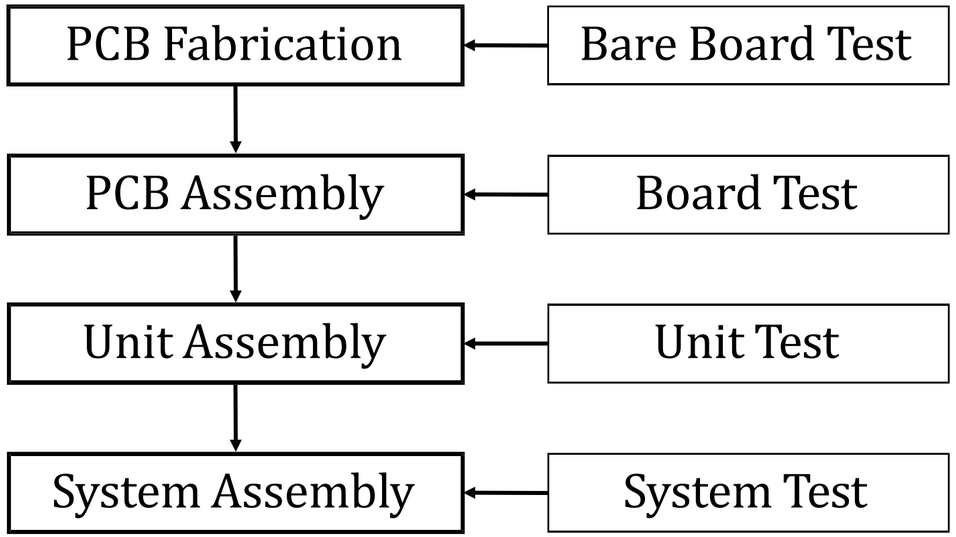
  - Catastrophic – due to random defects
  - Parametric – due to process variations
- Undesirable results during testing
  - Faulty chip appears to be good (passes test)
    - Called reject rate

$$reject\ rate = \frac{number\ of\ faulty\ parts\ passing\ final\ test}{total\ number\ of\ parts\ passing\ final\ test}$$

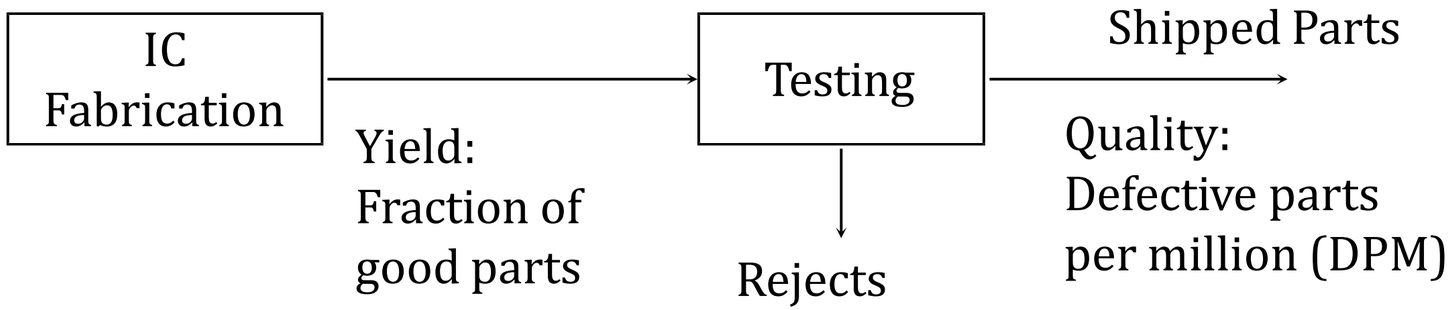
  - Good chip appears to be faulty (fails test)
    - Due to poorly designed tests or lack of DFT

ELECTRONIC SYSTEM MANUFACTURING

- A system consists of
  - PCBs that consist of
    - VLSI devices
- PCB fabrication similar to VLSI fabrication
  - Susceptible to defects
- Assembly steps also susceptible to defects
  - Testing performed at all stages of manufacturing



TESTING AND QUALITY



- Quality of shipped parts is a function of yield Y and the test (fault) coverage T
- Defect level (DL, reject rate in textbook): fraction of shipped parts that are defective

ASSESS MENT

1. How can you make test generation?
2. How can you generate random number?
3. List out the needs of testing
4. Define Yield and Reject Rate
5. Match all correctly

A 32-bit adder --- BIST

A 32-bit counter --- All test techniques

A 32MB Cache memory --- ATPG

A 10^7-transistor CPU --- Design for testability + ATPG

SUMMARY & THANK YOU