SNS COLLEGE OF ENGINEERING

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19EC505–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 4 –VLSI TESTING

TOPIC 3: MANUFACTURING TEST PRINCIPLES

OUTLINE

- Testing
  - –Logic Verification
  - –Silicon Debug
  - –Manufacturing Test
- Fault Models
- Activity
- Observability and Controllability
- Summary

TESTING-NEEDS

- Testing is one of the most expensive parts of chips
  - Logic verification accounts for > 50% of design effort for many chips
  - Debug time after fabrication has enormous opportunity cost
  - Shipping defective parts can sink a company

Example: Intel FDIV bug

- Logic error not caught until > 1M units shipped
- Recall cost $450M (!!!)

LOGIC VERIFICATION

- Does the chip simulate correctly?
  - Usually done at HDL level
  - Verification engineers write test bench for HDL
    - Can’t test all cases
    - Look for corner cases
    - Try to break logic design
- Ex: 32-bit adder
  - Test all combinations of corner cases as inputs:
    - 0, 1, 2, 2^{31}-1, -1, -2^{31}, a few random numbers
- Good tests require ingenuity

Silicon Debug

- Test the first chips back from fabrication
  - If you are lucky, they work the first time
  - If not…?????????
- Logic bugs vs. electrical failures
  - Most chip failures are logic bugs from inadequate simulation
  - Some are electrical failures
    - Crosstalk
    - Dynamic nodes: leakage, charge sharing
    - Ratio failures
  - A few are tool or methodology failures (e.g. DRC)
- Fix the bugs and fabricate a corrected chip

MANUFACTURING TEST

A speck of dust on a wafer is sufficient to kill chip

Yield of any chip is < 100%

Must test chips after manufacturing before delivery to customers to only ship good parts

Manufacturing testers are

very expensive

Minimize time on tester

Careful selection of

test vectors

TESTING YOUR CHIP

If you don’t have a multimillion dollar tester:

Build a breadboard with LED’s and switches

Hook up a logic analyzer and pattern generator Or use a low-cost functional chip tester

TESTOSTERICS

Ex: Testoster ICs functional chip tester

Designed by clinic teams and David Diaz at HMC

Reads your IRSIM test vectors, applies them to your chip, and reports assertion failures

STUCK-AT FAULTS

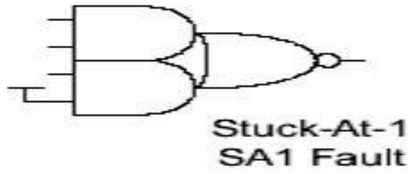
How does a chip fail?

- Usually failures are shorts between two conductors or opens in a conductor
- This can cause very complicated behavior

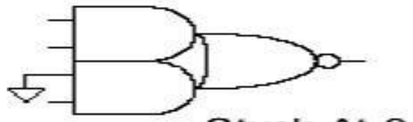
A simpler model: *Stuck-At*

- Assume all failures cause nodes to be “stuck-at” 0 or 1, i.e. shorted to GND or V_{DD}
- Not quite true, but works well in practice

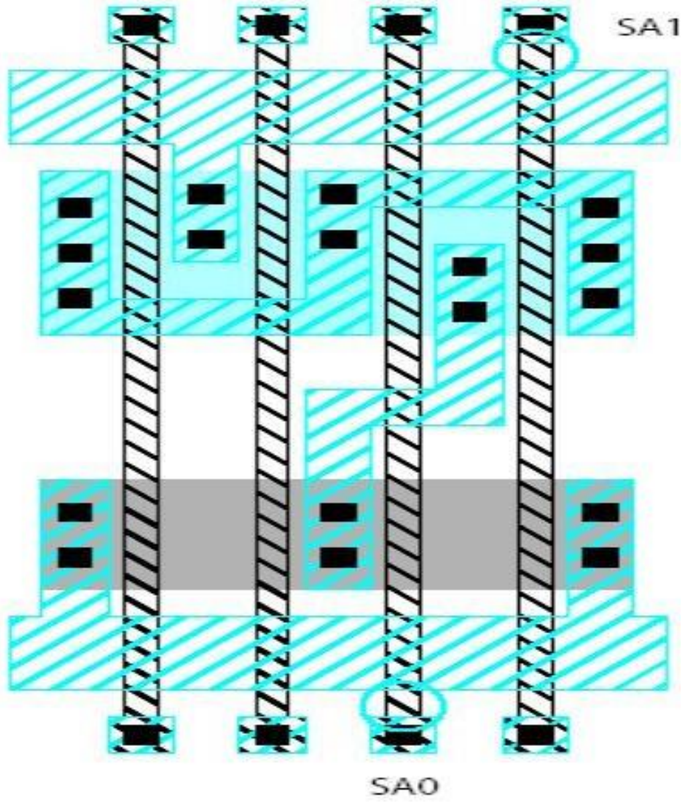
STUCK-AT FAULTS-EXAMPLES



Stuck-At-1
SA1 Fault



Stuck-At-0
SA0 Fault



ACTIVITY

SHAPE JOINING

LITY & CONTROLL ABILITY

Observability: ease of observing a node by watching external output pins of the chip

Controllability**:** ease of forcing a node to 0 or 1 by driving input pins of the chip

Combinational logic

-observe and control

-Finite state machines –difficult (requiring many cycles to enter desired state)

if state transition diagram is not known to the test engineer

TEST PATTERN GENERATION

- Manufacturing test ideally would check every node in the circuit to prove it is not stuck.
- Apply the smallest sequence of test vectors necessary to prove each node is not stuck.
- Good observability and controllability reduces number of test vectors required for manufacturing test.
  - Reduces the cost of testing
  - Motivates design-for-test

TEST EXAMPLE

	SA1	SA0
• A_3	{0110}	{1110}
• A_2	{1010}	{1110}
• A_1	{0100}	{0110}
• A_0	{0110}	{0111}
• n1	{1110}	{0110}
• n2	{0110}	{0100}
• n3	{0101}	{0110}
• Y	{0110}	{1110}

- Minimum set: {0100, 0101, 0110, 0111, 1010, 1110}

FABRICATION

Think about testing from the beginning

Simulate as you go

Plan for test after fabrication

“If you don’t test it, it won’t work!

(Guaranteed)”

ASSESSMENT

1. How can you test the Loaded materials weight in lorry Say with examples
2. Struck at fault 0 vs 1
3. List out the Testing Needs?
4. Any other Examples of Testing
5. Differentiate Observability & controllability

SUMMARY & THANK YOU