



# **SNS COLLEGE OF ENGINEERING**

**Kurumbapalayam (PO), Coimbatore – 641 107**

**Accredited by NAAC-UGC with 'A' Grade**

**Approved by AICTE, Recognized by UGC & Affiliated to Anna University, Chennai**

## **DEPARTMENT OF INFORMATION TECHNOLOGY**

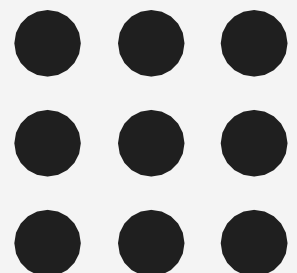
### **COURSE NAME: 23ITT201 DIGITAL PRINCIPLES AND**

### **COMPUTER ORGANIZATION**

### **II YEAR/ III SEM**

### **Unit 4 : PROCESSOR**

### **PIPELINE HAZARDS**





# PIPELINE HAZARDS

There are situations in pipelining when the next instruction cannot execute in the following clock cycle. These events are called *hazards*, and there are three different types.

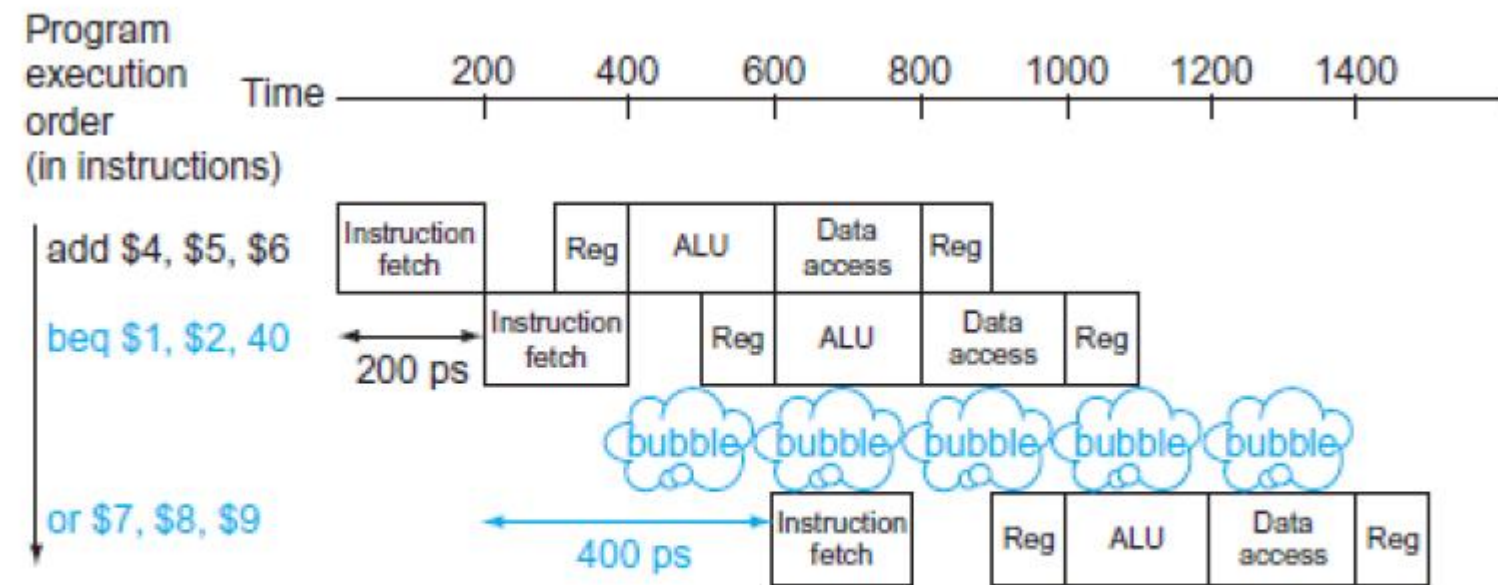
## Hazards

- Structural Hazards
- Data Hazards
- Control Hazards



## CONTROL HAZARDS

- ❖ It is also called as branch hazard. When the proper instruction cannot execute in the proper pipeline clock cycle because the instruction that was fetched is not the one that is needed; that is, the flow of instruction addresses is not what the pipeline expected.
- ❖ A control hazard, arising from the need to make a decision based on the results of one instruction while others are executing.



**FIGURE 3.18: Pipeline showing stalling on every conditional branch as solution to control hazards.**

- ❖ Even with this extra hardware, the pipeline involving conditional branches would look like figure 3.18. The lw instruction, executed if the branch fails, is stalled one extra 200 ps clock cycle before starting.
- ❖ The equivalent decision task in a computer is the branch instruction. Notice that we must begin fetching the instruction following the branch on the very next clock cycle.
- ❖ Nevertheless, the pipeline cannot possibly know what the next instruction should be, since it only just received the branch instruction from memory.



Thank You