Different Processors Questions

Latest Different Processors MCQ Objective Questions

Question 1:

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Match List I with List II:

List I (Communication Mode)		List II (Features)	
(A)	Mode 0	(I)	High speed; 8-bit shift register; one baud rate of f/12
(B)	Mode 1	(II)	Standard 8-bit UART; variable baud rate using time 1 overflows
(C)	Mode 2	(III)	Multiprocessor 9-bit UART: variable baud rate using time 1 overflows
(D)	Mode 3	(IV)	Multiprocessor 9-bit UART; two baud rates of f/32 and f/64

Choose the correct answer from the options given below:

1. (A) - (I), (B) - (II), (C) - (IV), (D) - (III)

2. (A) - (I), (B) - (II), (C) - (III), (D) - (IV)

3. (A) - (IV), (B) - (III), (C) - (I), (D) - (II)

4. (A) - (II), (B) - (III), (C) - (I), (D) - (IV)

Answer (Detailed Solution Below)

Option 1 : (A) - (I), (B) - (II), (C) - (IV), (D) - (III)

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Different Processors Question 1 Detailed Solution

Serial data transmission modes :

modes	bit UART	baud rate
mode 0	8 bit	(1/12 of the oscillator frequency)
mode 1	8 bit	variable and decided by timer 1
mode 2	9 bit	(1/32 or 1/64 of the oscillator frequency)
mode 3	9 bit	variable and decided by timer 1

option 1 is correct.

Question 2:

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After the execution of following program in 8051 microcontroller, the content in the accumulator will be

MOV R5, # 2AH

MOV R7, #C3H

MOVA, #R5

ADD A, #R7

ADD A, #10H

ADD A, #00H

1. 00H
2. EDH
3. 10H
4. FDH

Answer (Detailed Solution Below)

Option 4 : FDH

Different Processors Question 2 Detailed Solution

Concept

MOV R5, # 2AH

This command will transfer the content 2AH in the R5 register.

MOV R7, #C3H

This command will transfer the content C3H in the R7 register.

MOVA, #R5

This command will transfer the content of register R5 to the accumulator.

ADD A, #R7

This command will add the content of the accumulator with the content of register R7 and store the result in the accumulator.

2A + C3 = ED

∴ ED will be stored in the accumulator.

ADD A, #10H

This command will add the content of the accumulator with the 10 H

ED + 10H = FD

ADD A, #00H

FD + 00 = FD

Finally, the content in the accumulator will be FD H.

Question 3:

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Which of the following is/are NOT processor control instructions?

A. STC

B. CMC

C. JNO

D. NOP

E. CWD

Choose the correct answer from the options given below:

1. A, B and E only
2. C and E only
3. C and D only
4. D and E only

Answer (Detailed Solution Below)

Option 2 : C and E only

Different Processors Question 3 Detailed Solution

processor control instructions: It controls the processor's instructions by flag registers with set and reset.

These instructions are:

Instruction	Description
CLC	Clear carry flag
CLD	Clear direction flag
CLI	Clear interrupt flag
CMC	Complement the carry flag
STC	Set carry flag
STD	Set direction flag
STI	Set interrupt flag
HLT	Halt: it stops the execution of the program
NOP	No operation performs
ESC	Escape
WAIT	the processor enters an idle state

STC, CMC, and NOP are processor control instructions

JNO and CWD are not processor control instructions.

JNO instruction is jump if no overflow and CWD is to convert the signed word to a signed double word.

correct option is 2.

Question 4:

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If each core in a 16-core processor has a yield of 90% and nothing else on the chip fails. what is the yield of the chip ?

1. $(0.9)^8$
2. $(0.9)^{16}$
3. $(0.1)^8$
4. $(0.1)^{16}$

Answer (Detailed Solution Below)

Option 2 : $(0.9)^{16}$

Different Processors Question 4 Detailed Solution

The correct answer is **option 2.**

Key Points

A multi-core processor is a computer processor on a single integrated circuit with two or more separate processing units, called cores, each of which reads and executes program instructions.

Given that,

Number of core = 16-core

Processor yield = 90% (0.9)

Since there is no failure rate of the chip and as it is a 16-core processor with 90 % efficiency,

All the cores must work, therefore, the yield of the chip is $(0.9)^{16}$.

Hence the correct answer is $(0.9)^{16}$.

Question 5:

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Which one of the following characteristics is correct regarding RISC processor ?

1. Relatively very large addressing modes
2. Multi-cycle instruction execution
3. All operations are not done within the registers of the CPU
4. Relatively few instructions

Answer (Detailed Solution Below)

Option 4 : Relatively few instructions

Different Processors Question 5 Detailed Solution

Combinational logic units, which have a finite number of gates and can create specified outputs dependent on the instructions used to activate those responses, are used to implement hardwired control units. Their design is based on a fixed architecture, which requires wiring adjustments if the instruction set is updated or modified. In computers with a small instruction set, this design is

preferable (RISC).
The main idea is to simplify hardware by using an instruction set consisting of a few basic steps for loading, evaluating, and storing operations, similar to how a load command loads data and a store command stores it.
RISC processors provide very few addressing modes: often just one or two. A large Number of Registers: Since RISC processors use register-to-register operations, we need to have a large number of registers.

Characteristic of RISC –

1. Simpler instruction, hence simple instruction decoding.
2. Instruction comes undersize of one word.
3. Instruction takes a single clock cycle to get executed.
4. More general-purpose registers.
5. Simple Addressing Modes.
6. Fewer Data types.
7. The pipeline can be achieved.

RISC	CISC
Reduced Instruction Set Architecture	Complex Instruction Set Architecture
Focus on software	Focus on hardware
Uses only Hardwired control unit	Uses both hardwired and microprogrammed control unit
Transistors are used for more registers	Transistors are used for storing complex Instructions
Fixed sized instructions	Variable sized instructions
Can perform only Register to Register Arithmetic operations	Can perform REG to REG or REG to MEM or MEM to MEM
Requires more number of registers	Requires less number of registers
Code size is large	Code size is small
An instruction executed in a single clock cycle	Instruction takes more than one clock cycle

Top Different Processors MCQ Objective Questions

Question 6 View this Question Online >

An IC that transforms parallel data to serial in the asynchronous format and vice versa

1. UART
2. USART
3. MODEM
4. RS232C

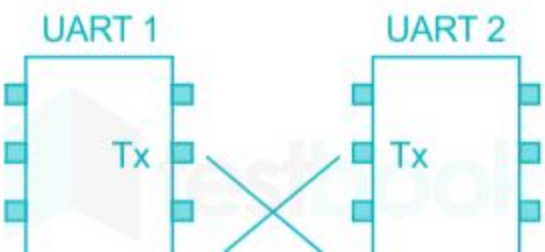
Answer (Detailed Solution Below)

Option 1 : UART

Different Processors Question 6 Detailed Solution

UART:

- UART stands for Universal Asynchronous Receiver/Transmitter. It's not a communication protocol like SPI and I2C, but a physical circuit in a microcontroller, or a stand-alone IC.
- **An IC that transforms parallel data to serial in the asynchronous format and vice versa is UART**
- A UART's main purpose is to transmit and receive serial data.
- In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controlling device like a CPU into serial form, transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving device.
- Only two wires are needed to transmit data between two UARTs. Data flows from the Tx pin of the transmitting UART to the Rx pin of the receiving UART:



Important Point

USART:

- USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is a microchip that provides the computer with the interface necessary for communication with modems and other serial devices.
- It has synchronous and asynchronous data transfer.
- IC 8251 : USART (Universal Synchronous and Asynchronous Receiver Transmitter)

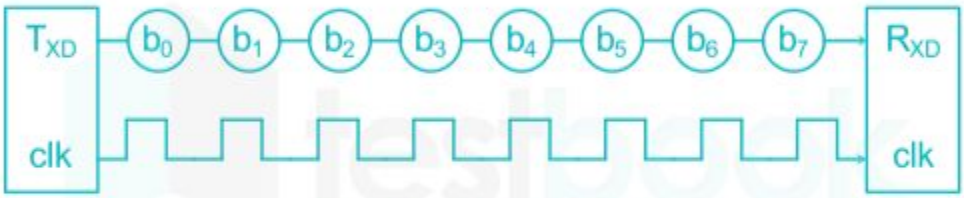
MODEM:

- A modem is a hardware device that allows a computer to send and receive data over a telephone line or a cable or satellite connection.
- **MODEM** stands for **modulator-demodulator**.
- A modem is used for transmitting and receiving data over a communication channel, such as twisted-pair telephone lines, coaxial cables, and optical fibers.
- At the source, the modulation technique is used to convert the analog signal to digital.
- At the receiver, demodulation is used to convert the digital signal back to analog.

RS232C:

- It is used for sending data sequentially over a computer bus through serial-bus communication.
- The date is transferred/transmitted bit by bit.
- It decides the data transmission rate.
- It establishes the way data is coded
- It defines signal voltage levels
- It defines standard connector configuration.

Serial communication is explained with the help of the following diagram:



Serial Communication

Question 7

View this Question Online >

The address size of 8086 microprocessor is

1. 4-bit
2. 8-bit
3. 16-bit
4. 20-bit

Answer (Detailed Solution Below)

Option 4 : 20-bit

Different Processors Question 7 Detailed Solution

For 8085 microprocessor:

1) Data or word size = 8 bits

2) Address = 16 bits

For 8086 microprocessor:

1) Data or word size = 16bit

2) Address = 20 bits

Question 8 View this Question Online >

RS232 is a

1. serial bus for data communication
2. parallel bus for data communication
3. MODEM
4. interrupt controller

Answer (Detailed Solution Below)

Option 1 : serial bus for data communication

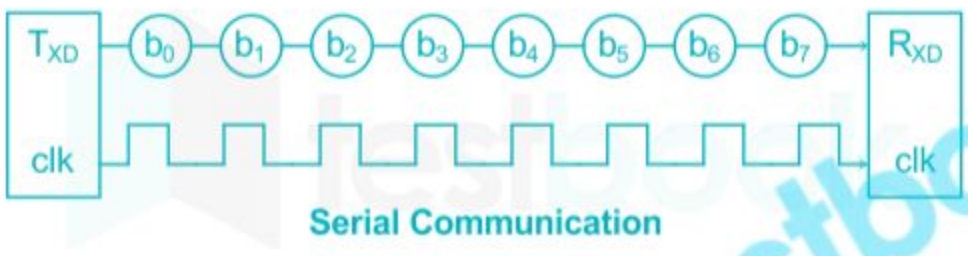
Different Processors Question 8 Detailed Solution

Serial bus Communication:

- It is a process of sending data sequentially over a computer bus is called as serial-bus communication.
- The date is transferred/transmitted bit by bit.

Ex **RS232**, RS449, RS485, RS422, RS429 etc

Serial communication is explained with the help of the following diagram:



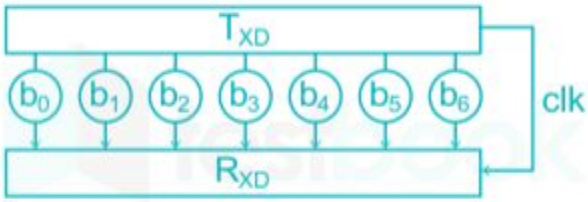
Serial Communication

Important Point

Parallel bus communication:

It is a process of sending data parallelly or transmitting in a byte or character on several data lines or buses at the same time.

This is explained as shown:



Parallel Bus Communication

Question 9

View this Question Online >

In PLC, FRD instruction does the following operation

1. Converts Integer value to BCD value
2. Converts HEX value to Binary value
3. Converts BCD value to HEX value
4. Converts BCD value to integer value

Answer (Detailed Solution Below)

Option 4 : Converts BCD value to integer value

Different Processors Question 9 Detailed Solution

Different Processors Question 9 Detailed Solution

- Programmable logic controllers or PLCs are digital computers used to perform control functions, usually for industrial applications.
- An instruction is a command that will cause a PLC to perform a certain predetermined operation.
- The instruction set for a particular PLC type lists the different types of instructions supported.
- The FRD command is an output command that is placed on the right side of the rung to **convert a BCD value from a source to an integer value** and place it into the destination when rung conditions are true.
- There are two values associated with this program, the Source and the Destination (Dest).
- The source and destination can be an address of a word (such as I:1, N7:0, T4:0).

An example is as shown:

Question 10 View this Question Online >

ARM processors were basically designed for _____.

1. Main frame systems
2. Distributed systems
3. Mobile systems
4. Super computers

Answer (Detailed Solution Below)

Option 3 : Mobile systems

Different Processors Question 10 Detailed Solution

- ARM stands for Advanced RISC Machines
- An ARM processor is any 16/32 bit microprocessor with **low electrical power consumption**, which makes them particularly **suitable for portable (mobile) systems**.
- ARM has got better performance when compared to other processors with low cost.
- ARM's assembly code is composed of many small instructions rather than less, but more complex instructions.

Question 11 View this Question Online >

TRAP flag in 8086 is used for

1. Single stepping
2. Increasing the speed of operation
3. Overflow detection
4. Calculation of physical address

Answer (Detailed Solution Below)

Option 1 : Single stepping

Different Processors Question 11 Detailed Solution

- Trap Flag (T) in 8086 is used for on-chip debugging.
- Setting the trap flag **puts the microprocessor into a single step mode** for debugging.
- In single stepping, the microprocessor executes an instruction and enters into a single step ISR.
- If the TRAP flag is set (1), the CPU automatically generates an internal interrupt after each instruction, allowing a program to be inspected as it executes instruction by the instruction.
- If the TRAP is reset (0), no function is performed.

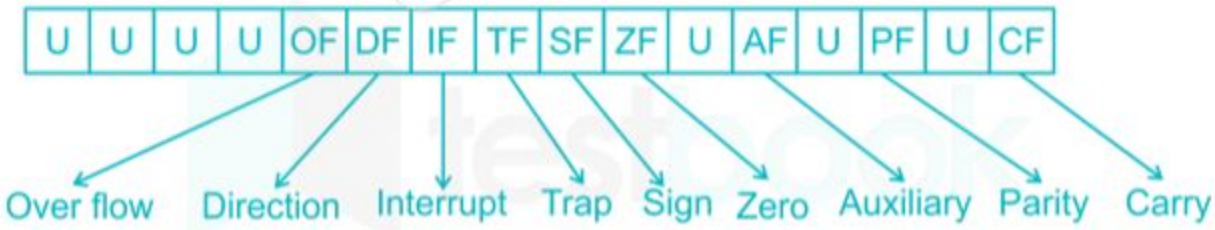
Important Point

8086 has 6 status flags which are:

Carry, Parity, Auxiliary Carry, Zero, Sign, and Overflow

8086 also has three control flags which are:

Direction, Interrupt Enable, and TRAP



TRAP flag is present in 8086 but not in 8085.

Question 12 View this Question Online >

SQL instruction in PLC is

1. An input instruction and used to monitor machine operating conditions
2. an output instruction and checks a sequencer file to control output devices.

3. An output instruction and captures reference conditions by manually stepping the machine through its operating sequences.

4. An input instruction and used for logic querying

Answer (Detailed Solution Below)

Option 3 : An output instruction and captures reference conditions by manually stepping the machine through its operating sequences.

Different Processors Question 12 Detailed Solution

Sequencer instructions are used to control automatic assembly machines that have a consistent and repeatable operation using 16-bit data.

Sequencer SQL (Sequencer Load):

- SQL is an output instruction used to capture reference conditions by manually stepping the machine through its operating sequences and loading I/O or storage data into destination files.
- It transfers data from the input source module to the sequencer file.
- The instruction functions much like a file-to-word transfer instruction.

Important Point

Sequencer Output (SQO): It is an output instruction that steps through a sequencer file of 16-bit output words whose bits have been set to control various output devices.

Sequencer Input (SQI): It is an input instruction used to monitor machine operating conditions for diagnostic purposes by comparing 16-bit image data through a mask, with data in a reference file.

Question 13 View this Question Online >

The concept of utilizing the bus for DMA operations is known as

1. CPU cheating
2. Cycle stealing
3. CPU stealing
4. None of these

Answer (Detailed Solution Below)

Option 2 : Cycle stealing

Different Processors Question 13 Detailed Solution

- Direct memory access (DMA) is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory, bypassing the CPU to speed up memory operations.
- The process is managed by a chip known as a DMA controller (DMAC).

Types of DMA transfer using a DMA controller:

- Burst or Block Transfer DMA
- Cycle Stealing or Single-Byte Transfer
- Transparent or Hidden DMA Transfer

Cycle Stealing Mode:

- In DMA's cycle stealing mode of operation, the DMA controller puts the CPU on hold for each byte of data to be transferred.
- In this mode, the DMA controller sends a HOLD signal to the microprocessor and waits for the HLDA signal.
- After receiving the HLDA signal, the **DMA controller gains control of the system bus** and executes only one DMA cycle.
- This concept of utilizing the bus for DMA operations is known as cycle stealing.

Question 14 View this Question Online >

The address space in ARM is _____

1. 2^{24}
2. 2^{8}
3. 2^{16}
4. 2^{32}

Answer (Detailed Solution Below)

Option 4 : 2^{32}

Different Processors Question 14 Detailed Solution

Concept:

Let a = number of address wires (width of the address bus)

d = number of data wires (width of the data bus)

The total addressed capacity(number of memory locations) in bytes is given by:

Memory Locations = 2^{a}

Observation:

- By increasing the width of the address bus, more memory locations can be directly addressed.
- Each time the width is increased by one wire, the address capacity is doubled.
- ARM processors normally have a 32-bit address bus.

- **A 32-bit ARM processor could address up to 2^{32}** memory locations, i.e. the addressable capacity is 2^{32} bytes (4 Gigabytes of memory)

Question 15 View this Question Online >

Which one of the following characteristics is correct regarding RISC processor ?

1. Relatively very large addressing modes
2. Multi-cycle instruction execution
3. All operations are not done within the registers of the CPU
4. Relatively few instructions

Answer (Detailed Solution Below)

Option 4 : Relatively few instructions

Different Processors Question 15 Detailed Solution

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Requires more number of registers	Requires less number of registers
Code size is large	Code size is small
An instruction executed in a single clock cycle	Instruction takes more than one clock cycle