SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

AN AUTONOMOUS INSTITUTION

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

Unit 4- PROCESSOR

Question Bank- 14 Marks

- **Explain the fetch-execute cycle in detail. Discuss the role of each component involved in the process.**

- **Compare and contrast hardwired control and microprogrammed control in a CPU. Discuss the advantages and disadvantages of each approach.**

- **Describe the structure of a basic CPU data path. Include diagrams to illustrate the flow of data during an arithmetic operation, and explain the function of each component.**

- **Discuss the concept of pipelining in processor design. Explain how pipelining increases instruction throughput and identify the challenges associated with implementing a pipelined architecture.**

- **Define and explain data hazards in pipelined processors. Provide examples of the three types of data hazards and discuss strategies to mitigate them.**

- **Explain control hazards and their impact on the performance of pipelined processors. Discuss techniques such as branch prediction and speculative execution to handle control hazards.**

- **Discuss the different stages of instruction execution in a pipelined architecture. Explain how these stages interact and the significance of each stage in terms of timing and data dependencies.**

- **Illustrate the concept of instruction-level parallelism (ILP). Discuss how modern processors exploit ILP and the techniques used to enhance performance, such as superscalar architecture and out-of-order execution.**

- **Describe the role of the control unit in a processor. Discuss how it generates control signals for various operations and the differences in control signal generation for hardwired and microprogrammed control units.**

- **Analyze the memory hierarchy in modern computer systems. Explain how the organization of memory affects CPU performance, discussing aspects like cache memory, virtual memory, and their respective roles in optimizing data access.**