SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF CSE (IoT)

COURSE NAME: 23ITT201 DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

II YEAR/ III SEM

Unit 4 : PROCESSOR

Pipelining

• Pipelining is an implementation technique in which multiple instructions are overlapped in execution.
• The computer pipeline is divided in stages.
• Each stage completes a part of an instruction in parallel.
• The stages are connected one to the next to form a pipe - instructions enter at one end, progress through the stages, and exit at the other end.

Today The non-pipelined approach to laundry would be as follows:

1. Place one dirty load of clothes in the washer.
2. When the washer is finished, place the wet load in the dryer.
3. When the dryer is finished, place the dry load on a table and fold.
4. When folding is finished, ask your roommate to put the clothes away.

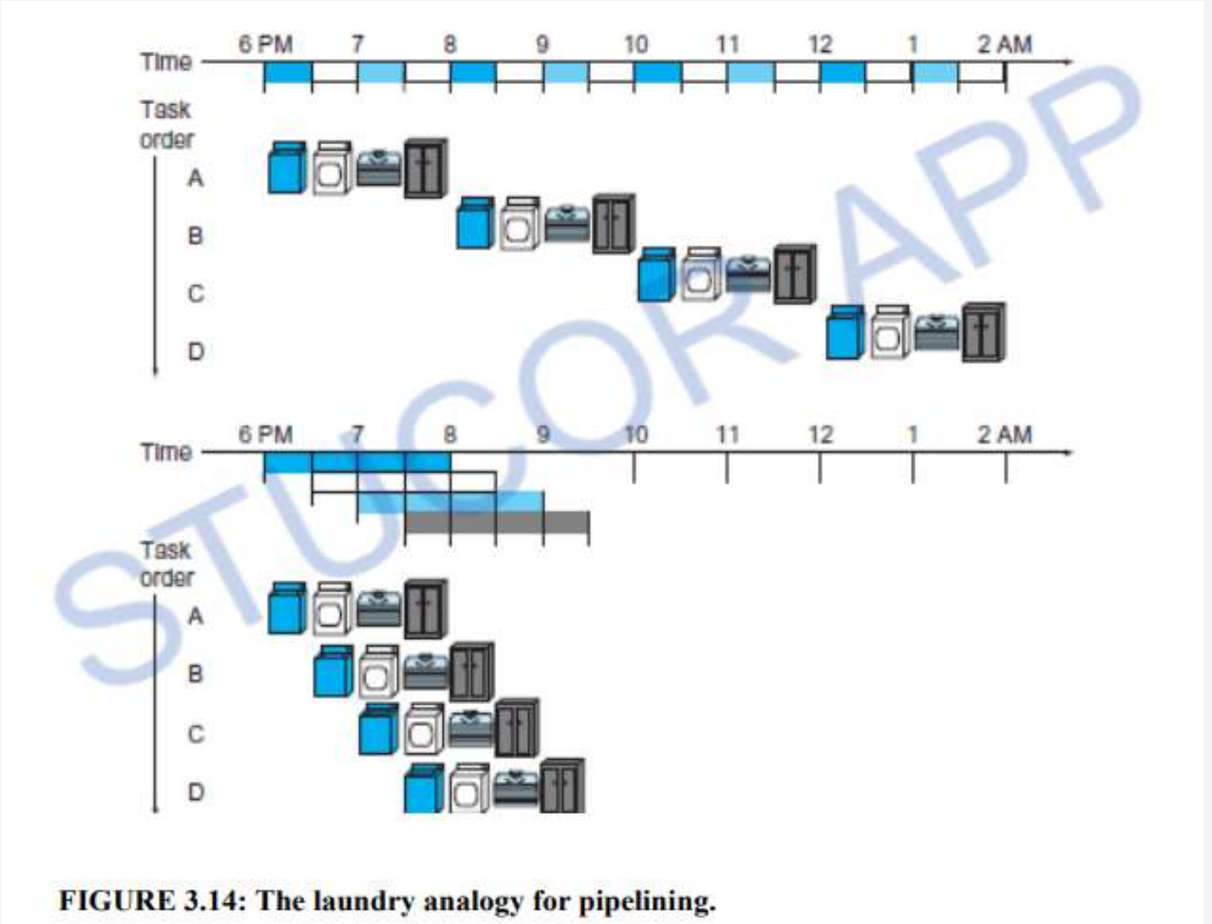

FIGURE 3.14: The laundry analogy for pipelining.

How Pipelines Works

❖ The pipeline is divided into segments and each segment can execute it operation concurrently with the other segments. Once a segment completes an operations, it passes the result to the next segment in the pipeline and fetches the next operations from the preceding segment.

❖ The pipelined approach takes much less time. As soon as the washer is finished with the first load and placed in the dryer, you load the washer with the second dirty load

The same principles apply to processors where we pipeline instruction-execution.

MIPS instructions classically take five steps:

1.Fetch instruction from memory.
2. Read registers while decoding the instruction. The regular format of MIPS instructions allows reading and decoding to occur simultaneously.
3. Execute the operation or calculate an address.
4. Access an operand in data memory.
5. Write the result into a register.

❖ First, all MIPS instructions are the same length. This restriction makes it much easier to fetch instructions in the first pipeline stage and to decode them in the second stage.

❖ Second, MIPS have only a few instruction formats, with the source register fields being located in the same place in each instruction. This symmetry means that the second stage can begin reading the register file at the same time that the hardware is determining what type of instruction was fetched

. ❖ Third, memory operands only appear in loads or stores in MIPS. This restriction means we can use the execute stage to calculate the memory address and then access memory in the following stage.

❖ Fourth, operands must be aligned in memory. Hence, we need not worry about a single data transfer instruction requiring two data memory accesses; the requested data can be transferred between processor and memory in a single pipeline stage.

Thank You