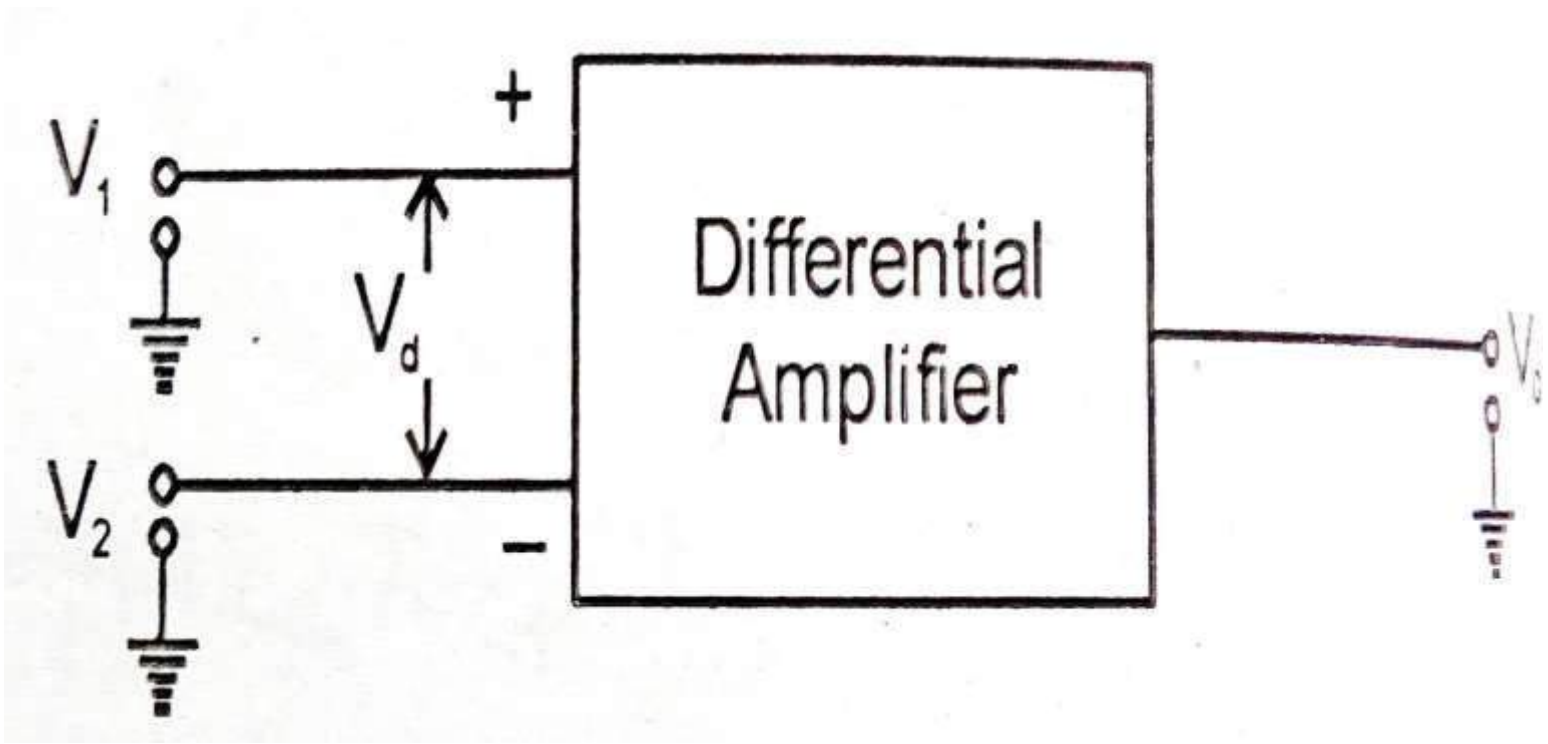
Analog Circuits
Day-10

Differential Amplifiers

Introduction

- The function of differential amplifier is to *amplify the difference of two signals.*
- The need for differential amplifier in many physical measurements arises where response from d.c to many megahertz is required. It is also the *basic input stage of an integrated amplifier.*

Block diagram of differential amplifier



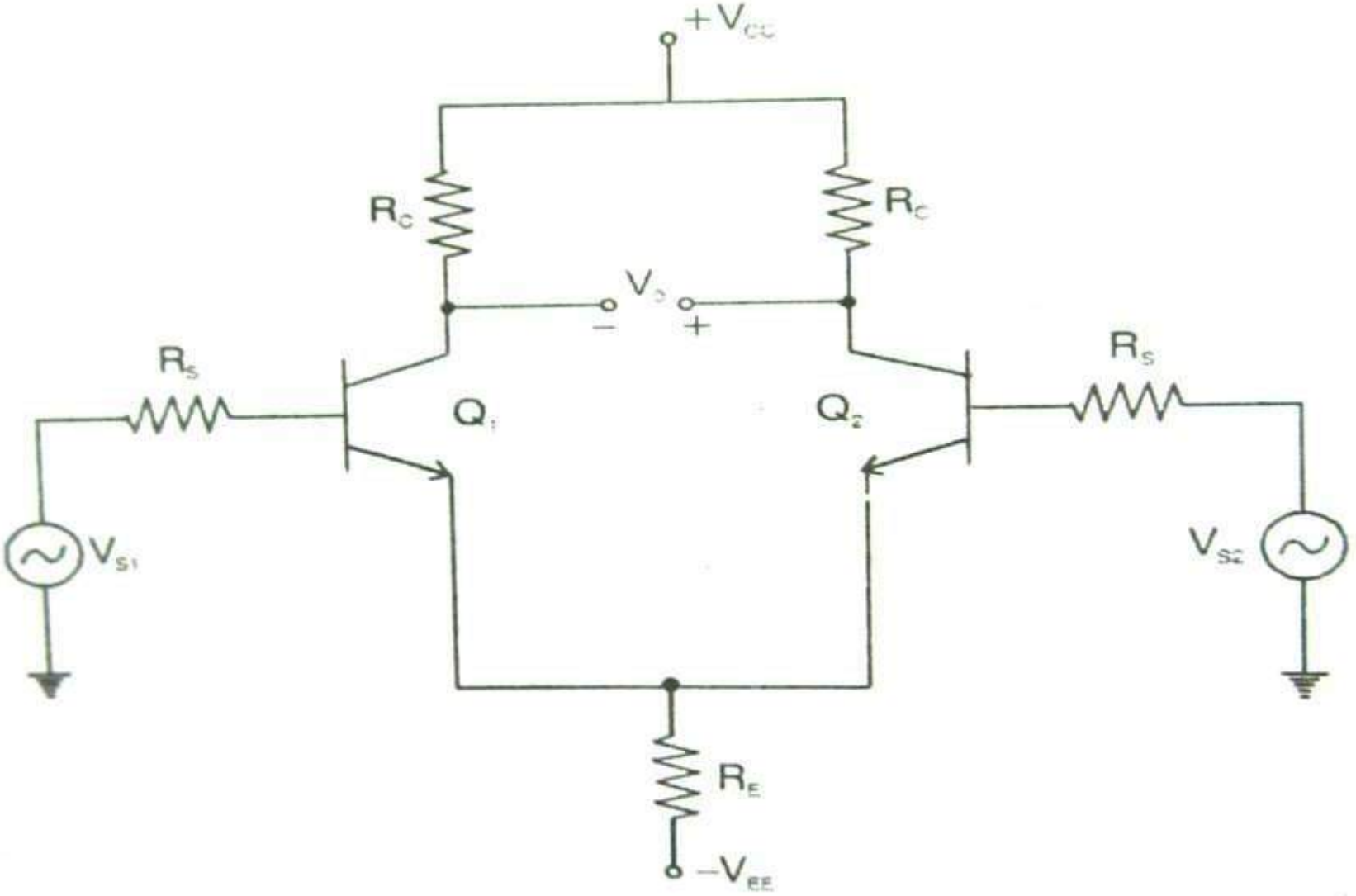


Fig. Basic configuration of a differential amplifier

- The output signal in a differential amplifier is proportional to the difference between the two input signals.

$$\mathbf{V_o \, \alpha \, (V_1 - V_2)}$$

Where,

$\mathbf{V_1}$ **&** $\mathbf{V_2}$ – Two input signals

$\mathbf{V_o}$ – Single ended output

Differential Gain (A_d):

$$V_o = A_d \ (V_1 - V_2)$$

Where, $\mathbf{A_d}$ is the **constant of proportionality**.

$\mathbf{A_d}$ is the gain with which differential amplifier amplifies the difference of two input signals.

Hence it is known as '***differential gain of the differential amplifier***'.

$$A_d = \frac{V_o}{V_d} = -g_m R_C$$

V_1-V_2= Difference of two voltage

Common Mode Gain (A_d):

An average of the two input signals is called common mode signal denoted as V_c.

$$V_c = \frac{V_1 + V_2}{2}$$

Hence, the differential amplifier also produces the output voltage proportional to common mode signals.

$$\mathbf{V_o = A_c V_c}$$

Where $\mathbf{A_c = - R_C / R_E}$, is the common mode gain.

Therefore, there exists some finite output for $V_1 = V_2$ due to common mode gain Ac.

Hence the total output of any differential amplifier can be given as,

$$\mathbf{V_o = A_d V_d + A_c V_c}$$

Common Mode Rejection Ratio (CMRR):

- The ability of a differential amplifier to reject a common mode signal is defined by a ratio called '***Common Mode Rejection Ratio***' denoted as CMRR.
- **CMRR** is defined as the ***ratio of the differential voltage gain A_d to common mode gain A_c*** and is expresses in dB.

$$\mathbf{CMRR = Ad/Ac = {}^{g}{}_{m}R_{E}}$$

$$CMRR = 20 \log \left| \frac{A_d}{A_c} \right| dB$$

Input and Output Resistances:

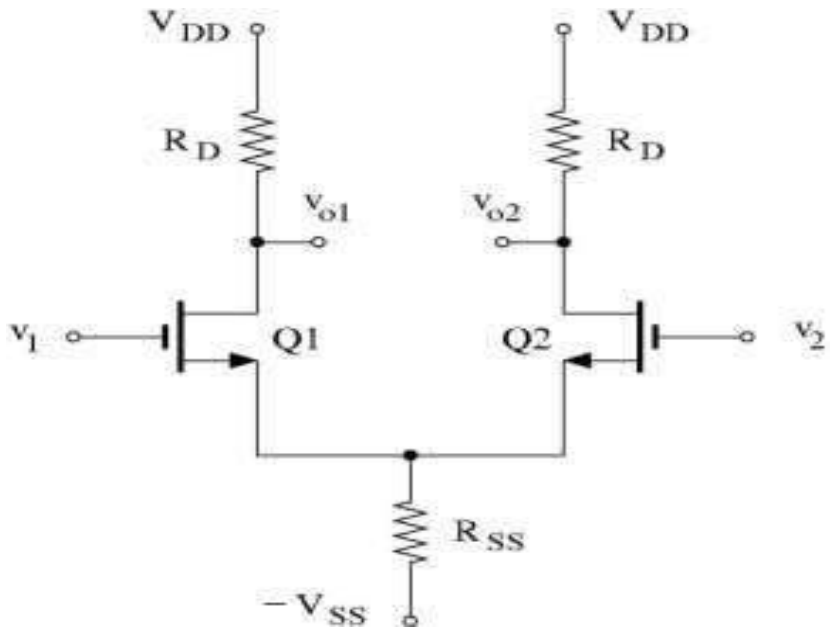
Diff. mode input resistance:

$R_i = 2\,r_e$

Diff. mode output resistance:

$R_o = R_C \;//\; r_o$

Differential Amplifier using FETs:



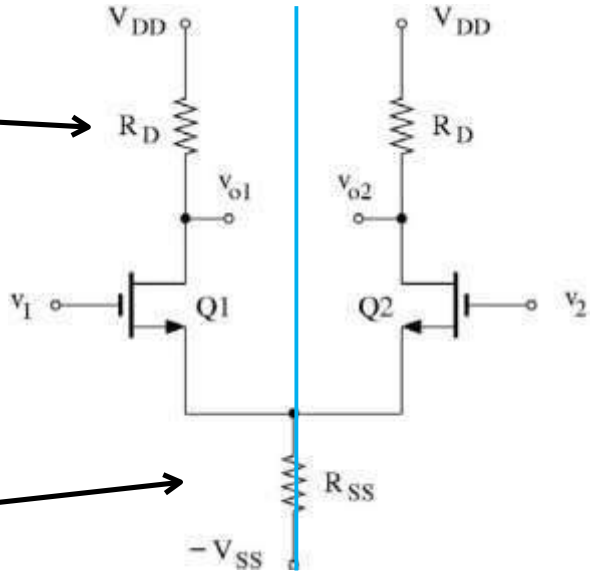
$$A_d = - {}^{g}{}_{m} R_D$$

$$A_c = - R_D / R_{ss}$$

$$CMRR = Ad/Ac = {}^{g}{}_{m} R_{ss}$$

- Identical transistors.
- Circuit elements are symmetric about the mid-plane.
- Identical bias voltages at Q1 & Q2 gates ($V_{G1} = V_{G2}$).
- Signal voltages & currents are different because $v_1 \neq v_2$.

Load R_D: resistor, current-mirror, active load, …



R_{SS}: Bias resistor, current source (current-mirror)

Q1 & Q2 are in CS-like configuration (input at the gate, output at the drain) but with sources connected to each other.

- For now, we keep track of "two" output, v_{o1} and v_{o2} , because there are several ways to configure "one" output from this circuit.

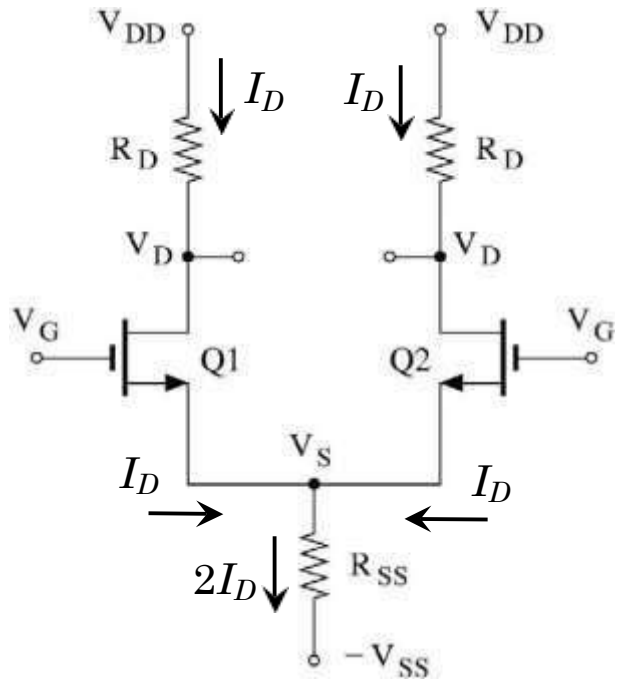
Since $V_{G1} = V_{G2} = V_G$

and $V_{S1} = V_{S2} = V_S$

$$V_{GS1} = V_{GS2} = V_{GS}$$
$$V_{OV1} = V_{OV2} = V_{OV}$$
$$I_{D1} = I_{D2} = I_D$$
$$V_{DS1} = V_{DS2} = V_{DS}$$

Also:

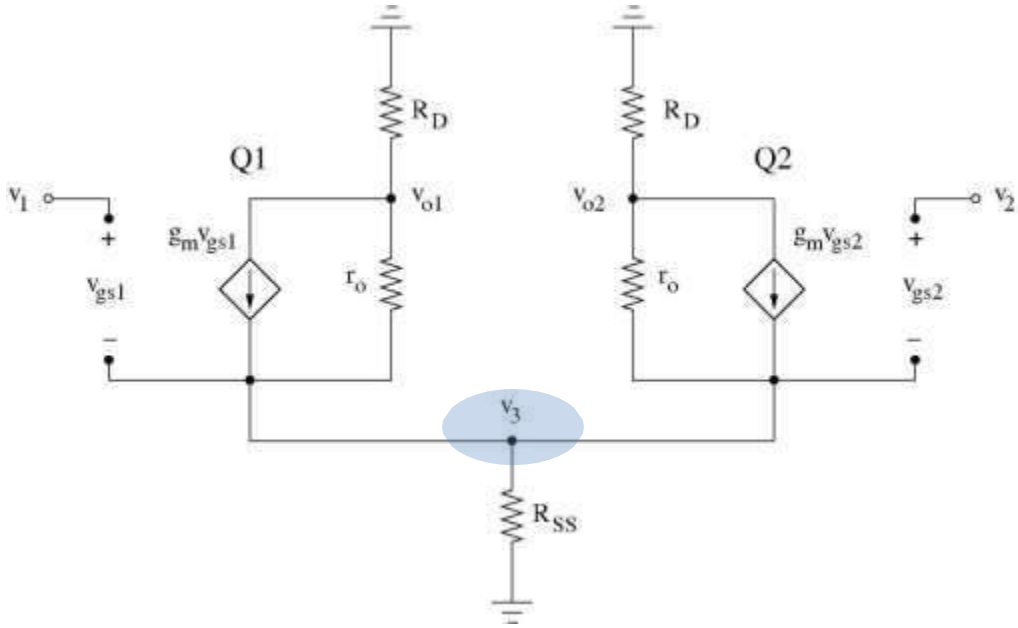
$$g_{m1} = g_{m2} = g_m$$
$$r_{o1} = r_{o2} = r_o$$



Differential Amplifier – Gain

$$v_{gs1} = v_1 - v_3$$

$$v_{gs\,2} = v_2 - v_3$$



Node Voltage Method:

Node v_{o1}: $\dfrac{v_{o1}}{R_D} + \dfrac{v_{o1} - v_3}{r_o} + g_m(v_1 - v_3) = 0$

Node v_{o2}: $\dfrac{v_{o2}}{R_D} + \dfrac{v_{o\,2} - v_3}{r_o} + g_m(v_2 - v_3) = 0$

Node v_3: $\dfrac{v_3}{R_{SS}} + \dfrac{v_3 - v_{o\,2}}{r_o} + \dfrac{v_3 - v_{o1}}{r_o} - g_m(v_1 - v_3) - g_m(v_2 - v_3) = 0$

Above three equations should be solved to find v_{o1}, v_{o2} and v_3 (lengthy calculations)

- **Because the circuit is symmetric, differential/common-mode method is the preferred method to solve this circuit (and we can use fundamental configuration formulas).**

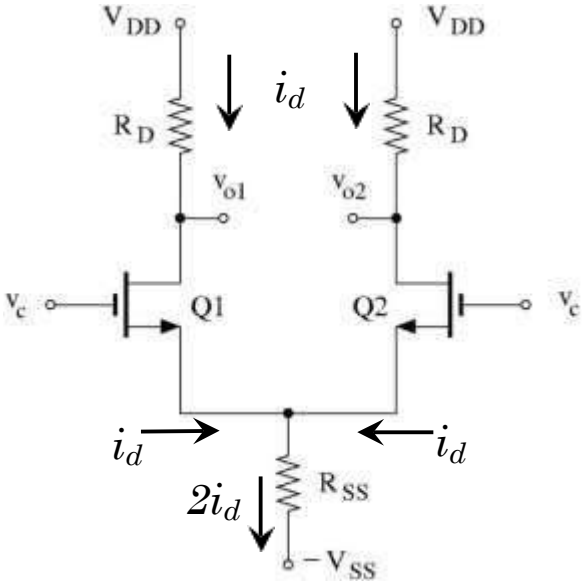
Differential Amplifier – Common Mode (1)

Common Mode: Set $v_d = 0$ (or set $v_1 = +v_c$ and $v_2 = +v_c$)

Because of summery of
the circuit and input signals*:

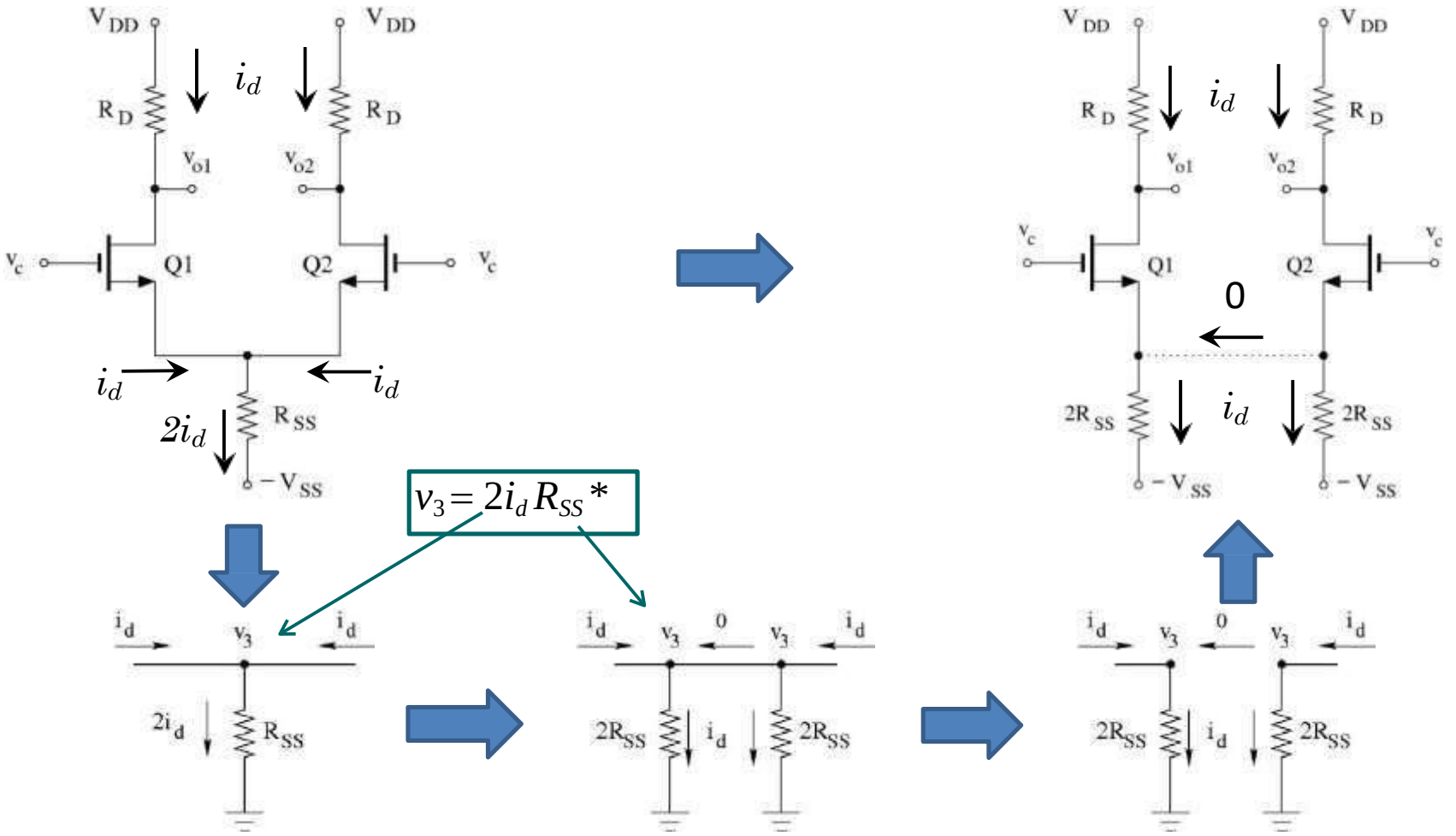
$$v_{o1} = v_{o2} \quad \text{and} \quad i_{d1} = i_{d2} = i_d$$

We can solve for v_{o1} by node voltage method but there is a simpler and more elegant way.



* If you do not see this, set $v_1 = v_2 = v_c$ in node equations of the previous slide, subtract the first two equations to get $v_{o1} = v_{o2}$. Ohm's law on R_D then gives $i_{d1} = i_{d2} = i_d$

Differential Amplifier – Common Mode (2)

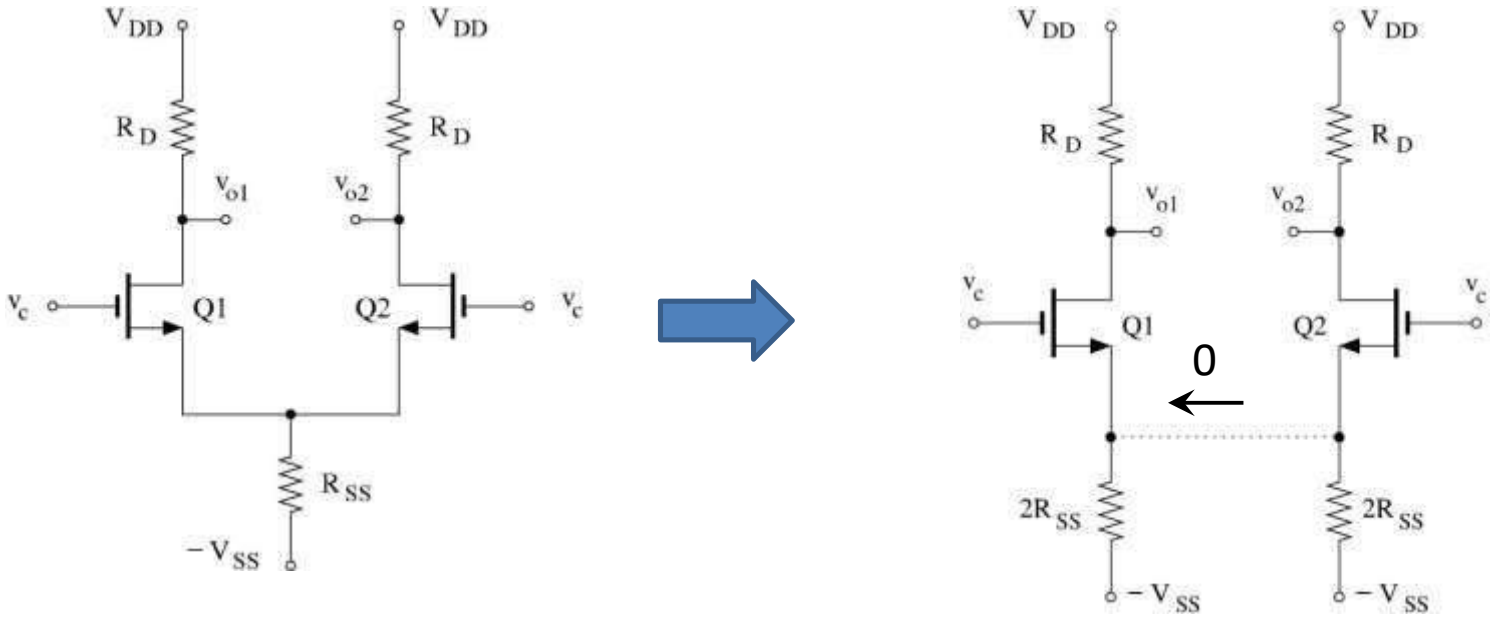


- **Because of the symmetry, the common-mode circuit breaks into two identical "half-circuits".**

* V_{ss} is grounded for signal

Differential Amplifier – Common Mode (3)

- **The common-mode circuit breaks into two identical half-circuits.**



CS Amplifiers with Rs

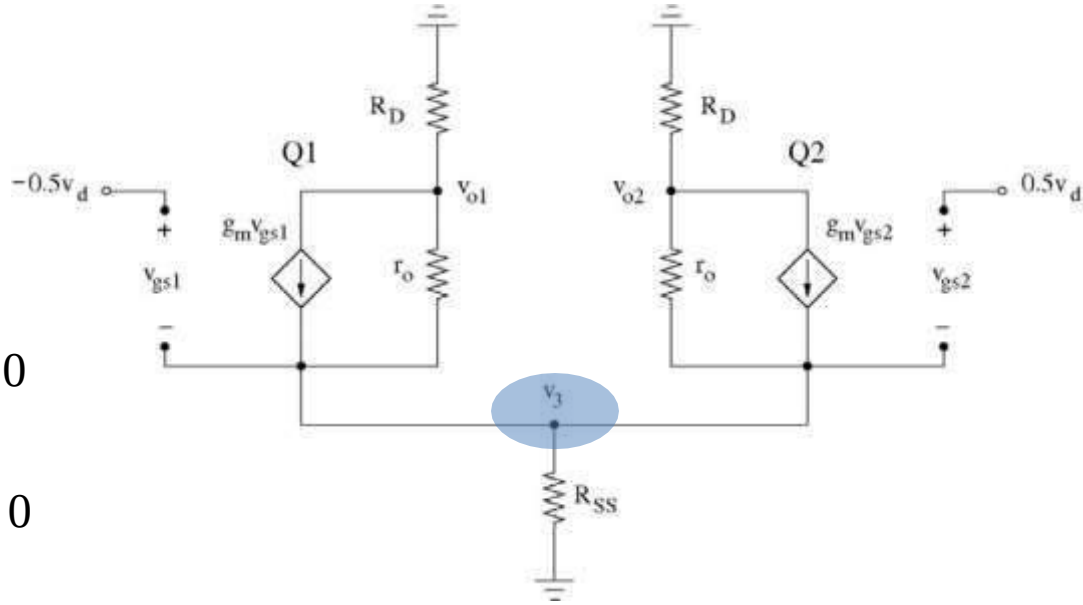
$$\frac{v_{o1}}{v_c} = \frac{v_{o2}}{v_c} = -\frac{g_m R_D}{1 + 2 g_m R_{SS} + R_D / r_o}$$

Differential Amplifier – Differential Mode (1)

Differential Mode: Set $v_c = 0$ (or set $v_1 = -v_d/2$ and $v_2 = +v_d/2$)

$$v_{gs1} = -0.5v_d - v_3$$

$$v_{gs2} = +0.5v_d - v_3$$



Node Voltage Method:

Node v_{o1}: $$\frac{v_{o1}}{R_D} + \frac{v_{o1} - v_3}{r_o} + g_m(-0.5v_d - v_3) = 0$$

Node v_{o2}: $$\frac{v_{o2}}{R_D} + \frac{v_{o2} - v_3}{r_o} + g_m(+0.5v_d - v_3) = 0$$

Node v_3: $$\frac{v_3}{R_{SS}} + \frac{v_3 - v_{o2}}{r_o} + \frac{v_3 - v_{o1}}{r_o} - g_m(-0.5v_d - v_3) - g_m(+0.5v_d - v_3) = 0$$

Node v_{o1} + Node v_{o2} : $$\left(\frac{1}{R_D} + \frac{1}{r_o}\right)(v_{o1} + v_{o2}) - \left(\frac{2}{r_o} + 2g_m\right)v_3 = 0$$

Node v_3: $$-\frac{1}{r_o}(v_{o1} + v_{o2}) + \left(\frac{1}{R_{SS}} + \frac{2}{r_o} - 2g_m\right)v_3 = 0$$

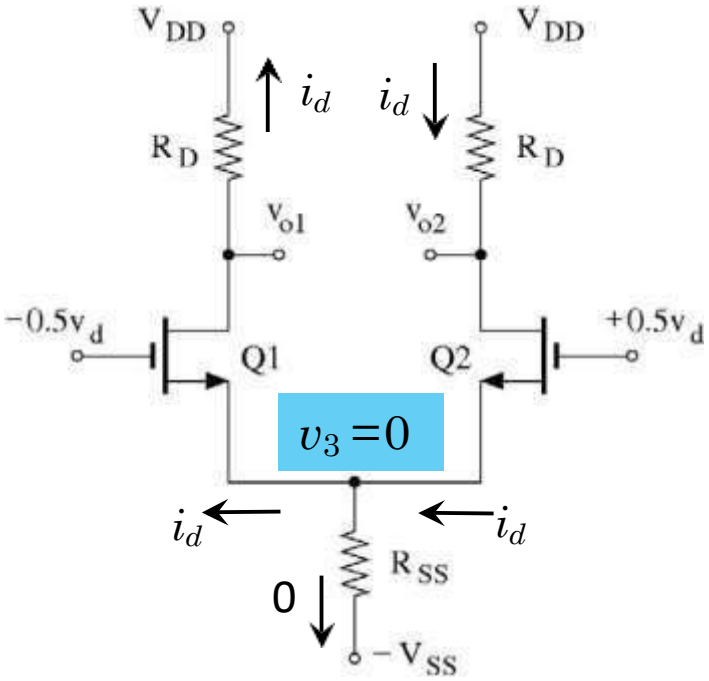
Only possible solution:

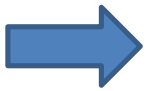
$$v_{o1} + v_{o2} = 0 \Rightarrow v_{o1} = -v_{o2}$$

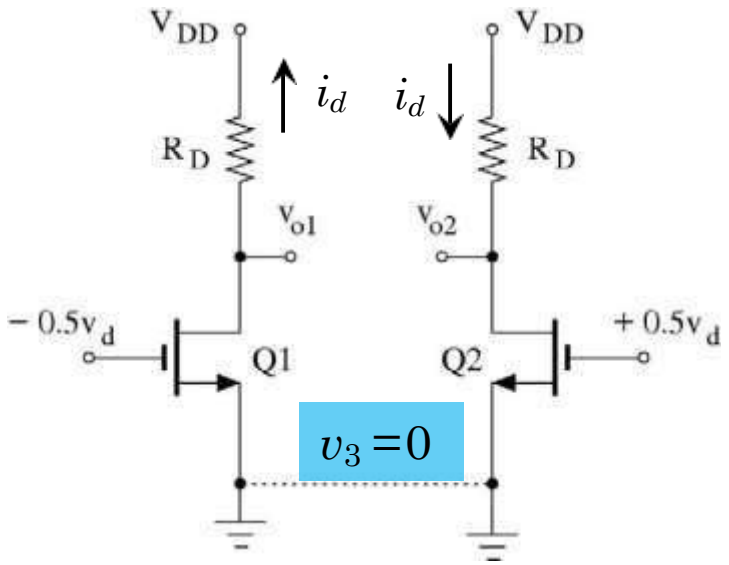
$$v_3 = 0$$

Differential Amplifier – Differential Mode (2)

$$v_3 = 0 \quad \text{and} \quad v_{o1} = -v_{o2} \quad \Rightarrow \quad i_{d1} = -i_{d2}$$







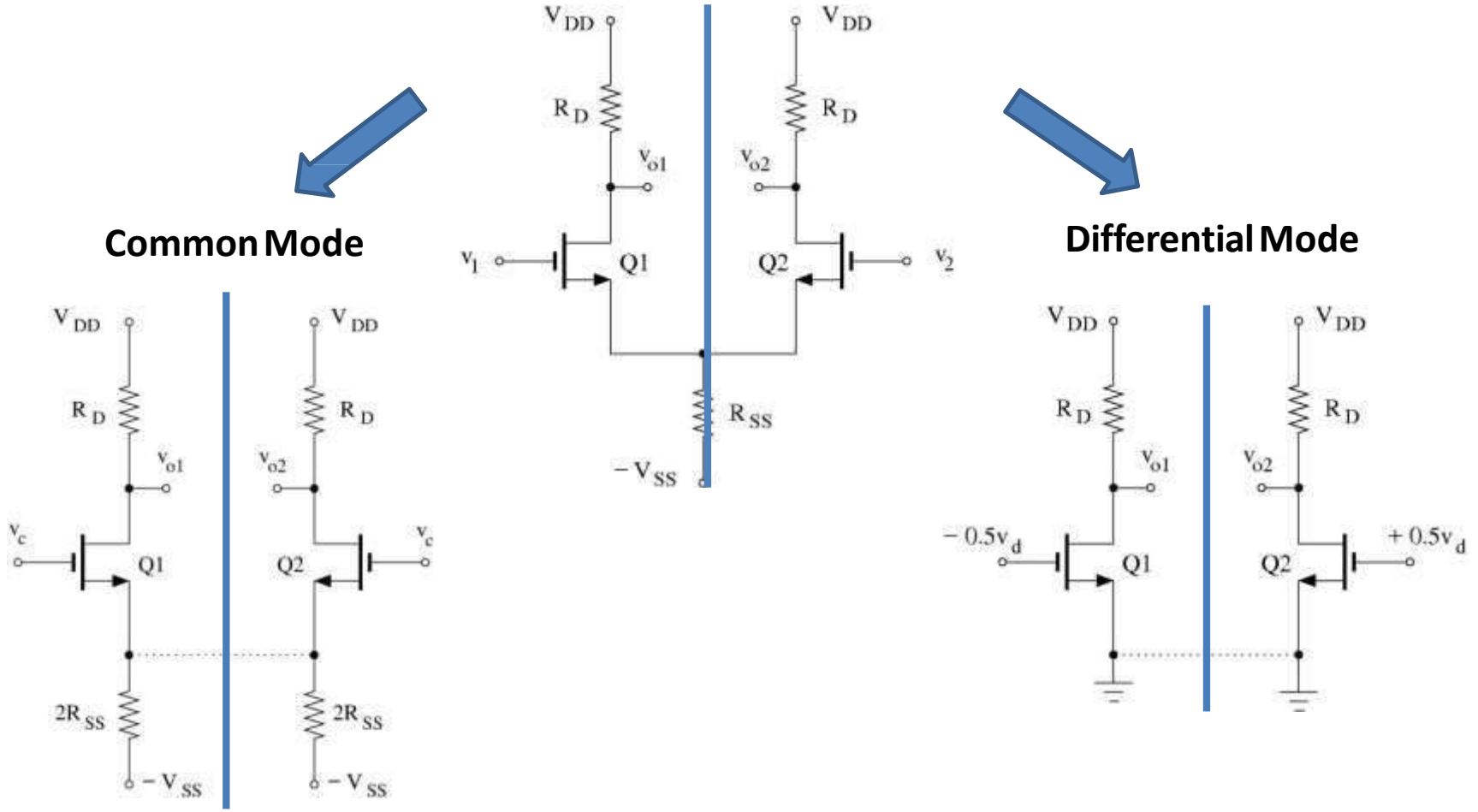
CS Amplifier

$$\frac{v_{o1}}{-0.5v_d} = -g_m(r_o \| R_D), \quad \frac{v_{o2}}{+0.5v_d} = -g_m(r_o \| R_D)$$

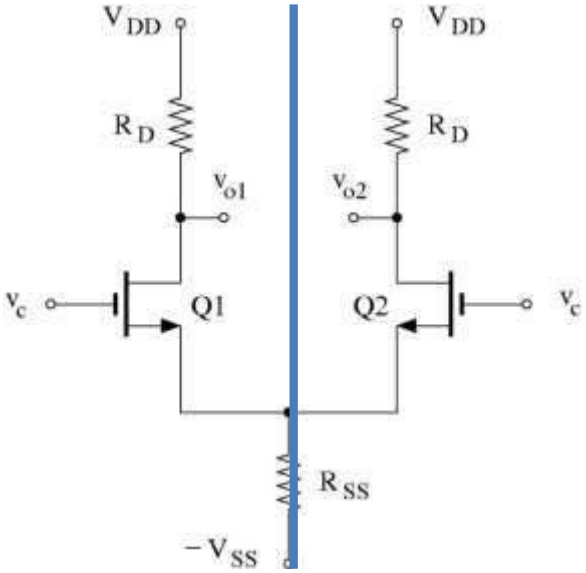
- **Because of the symmetry, the differential-mode circuit also breaks into two identical half-circuits.**

Concept of "Half Circuit"

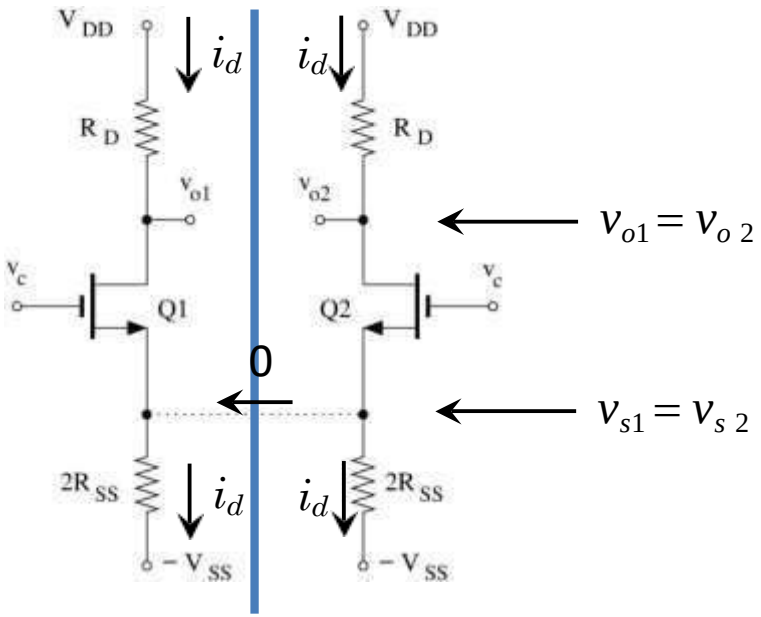
- For a symmetric circuit, differential- and common-mode analysis can be performed using "half-circuits."



Common-Mode "Half Circuit"



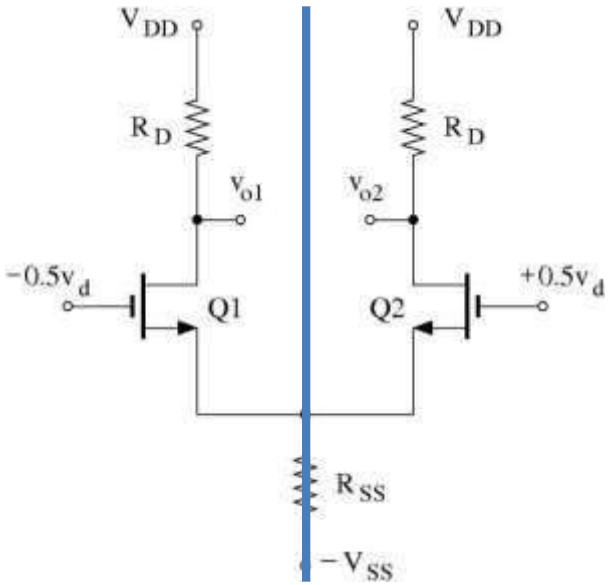
Common Mode circuit



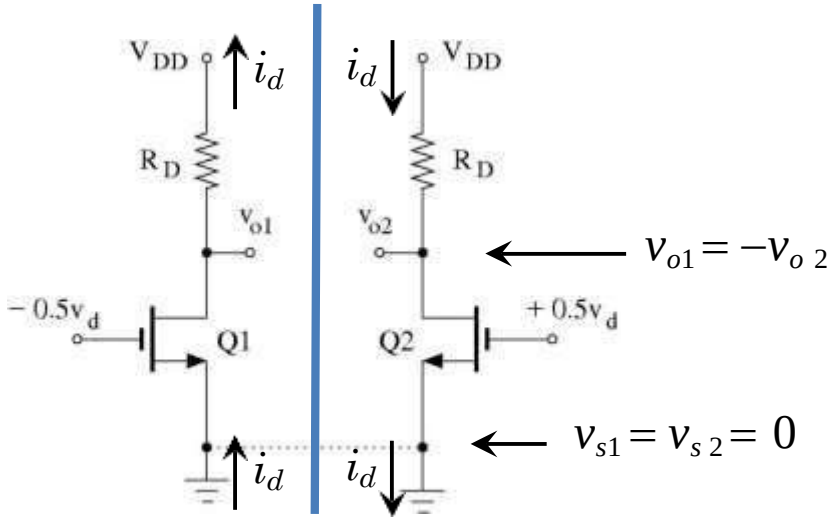
Common Mode Half-circuit

1. Currents about symmetry line are equal.
2. Voltages about the symmetry line are equal (e.g., $v_{o1} = v_{o2}$)
3. No current crosses the symmetry line.

Differential-Mode "Half Circuit"



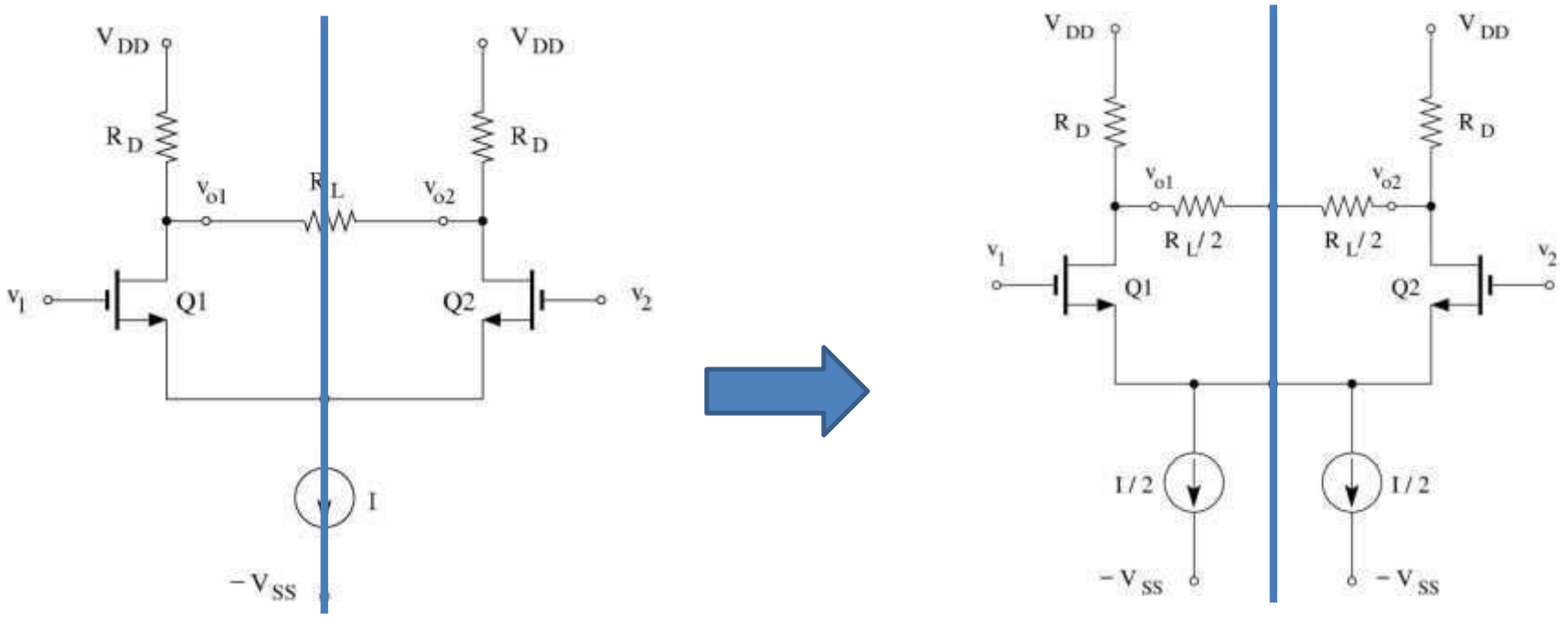
Differential Mode circuit



Differential Mode Half-circuit

1. Currents about the symmetry line are equal in value and opposite in sign.
2. Voltages about the symmetry line are equal in value and opposite in sign.
3. Voltage at the summery line is zero

Constructing "Half Circuits"



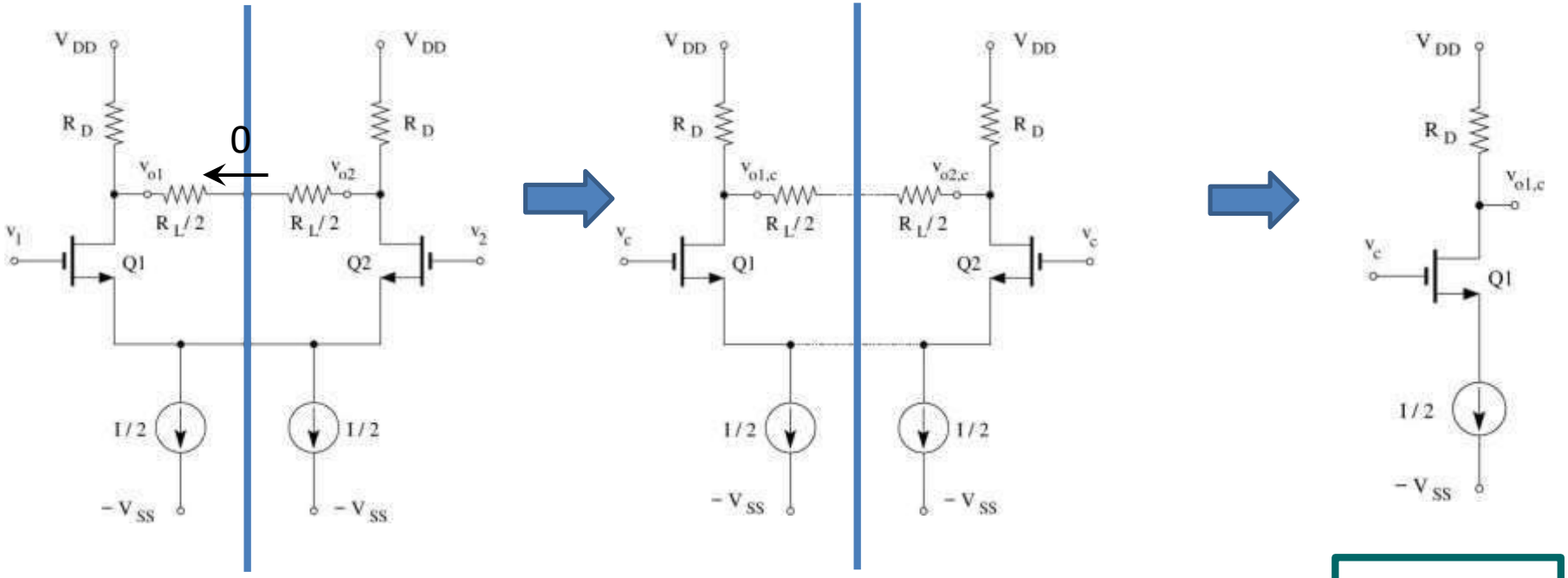
Step 1:

Divide **ALL elements** that <u>cross</u> the symmetry line (e.g., R_L) and/or <u>are located on</u> the symmetry line (current source) such that we have a symmetric circuit (only wires should cross the symmetry line, nothing should be located on the symmetry line!)

Constructing "Half Circuit"– Common Mode

Step 2: Common Mode Half-circuit

1. Currents about symmetry line are equal (e.g., $i_{d1} = i_{d2}$).
2. Voltages about the symmetry line are equal (e.g., $v_{o1} = v_{o2}$).
3. **No current crosses the symmetry line.**

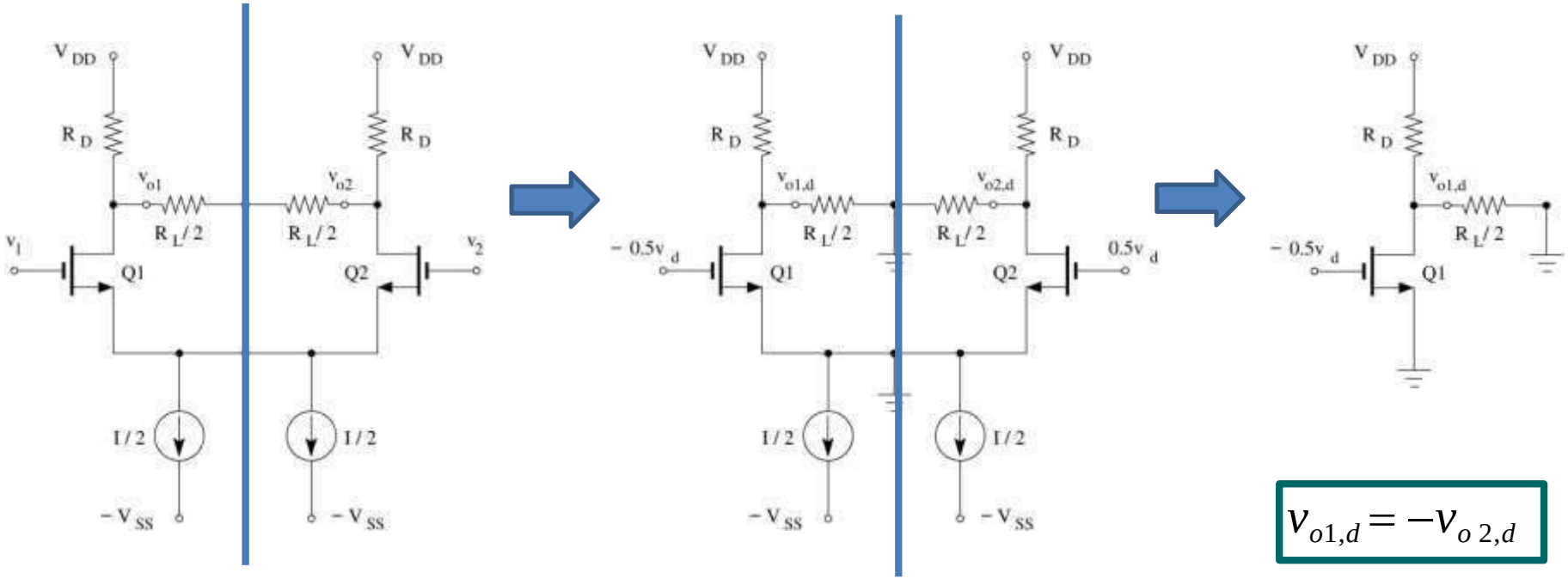


$v_{o1,c} = v_{o2,c}$

Constructing "Half Circuit"– Differential Mode

Step 3: Differential Mode Half-Circuit

1. Currents about symmetry line are equal but opposite sign (e.g., $i_{d1} = -i_{d2}$)
2. Voltages about the symmetry line are equal but opposite sign (e.g., $v_{o1} = -v_{o2}$)
3. **Voltage on the symmetry line is zero.**



$$v_{o1,d} = -v_{o\,2,d}$$

"Half-Circuit" works only if the circuit is symmetric !

- Half circuits for common-mode and differential mode are different.
- Bias circuit is similar to Half circuit for common mode.
- Not all difference amplifiers are symmetric. Look at the load carefully!

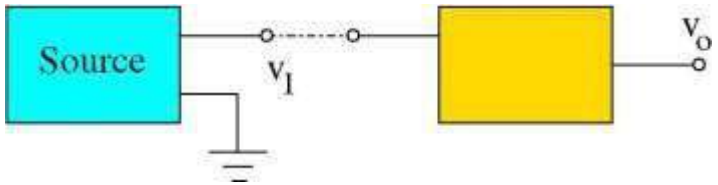
- We can still use half circuit concept if the deviation from prefect symmetry is small (i.e., if one transistor has R_D and the other $R_D + \Delta R_D$ with $\Delta R_D << R_D$).
  - However, we need to solve BOTH half-circuits (see slide 30)

Why are Differential Amplifiers popular?

- **They are much less sensitive to noise (CMRR >>1).**
- Biasing: Relatively easy direct coupling of stages:
  - Biasing resistor (R_{SS}) does not affect the differential gain (and does not need a by-pass capacitor).
  - No need for precise biasing of the gate in ICs
  - DC amplifiers (no coupling/bypass capacitors).
- …

Why is a large CMRR useful?

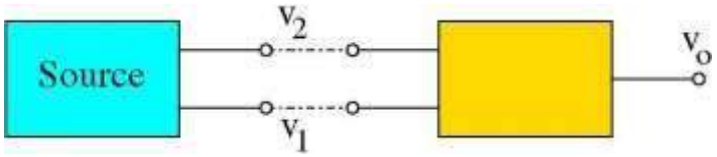
- A major goal in circuit design is to minimize the noise level (or improve signal-to-noise ratio). Noise comes from many sources (thermal, EM, …)
- A regular amplifier "amplifies" both signal and noise.



$$v_1 = v_{sig} + v_{noise}$$

$$v_o = A \cdot v_1 = A \cdot v_{sig} + A \cdot v_{noise}$$

- However, if the signal is applied between two inputs and <u>we use a difference amplifier with a large CMRR</u>, the signal is amplified a lot more than the noise which improves the signal to noise ratio.*



$$v_1 = -0.5v_{sig} + v_{noise} \;\&\; v_2 = +0.5v_{sig} + v_{noise}$$

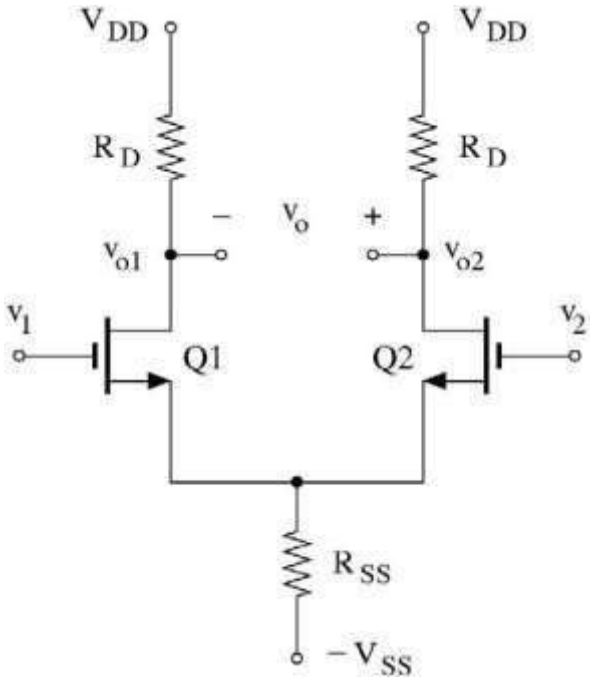
$$v_d = v_2 - v_1 = v_{sig} \qquad \& \; v_c = v_{noise}$$

$$v_o = A_d \cdot v_d + A_c \cdot v_c = A_d \cdot v_{sig} + \frac{A_d}{CMRR} \cdot v_{noise}$$

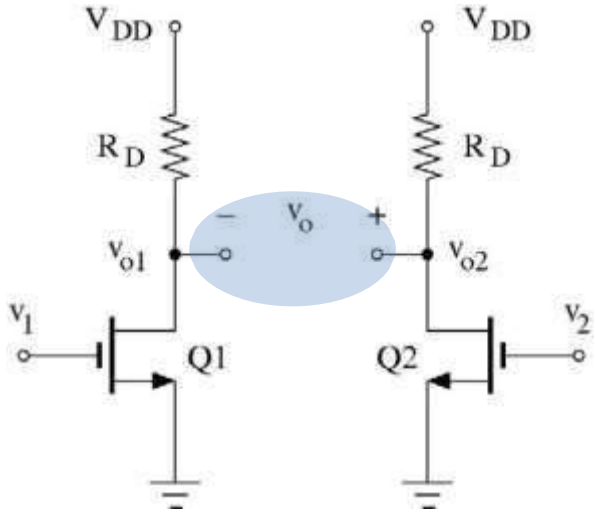
* Assuming that noise levels are similar to both inputs.

Comparing a differential amplifier two identical CS amplifiers (perfectly matched)

Differential Amplifier



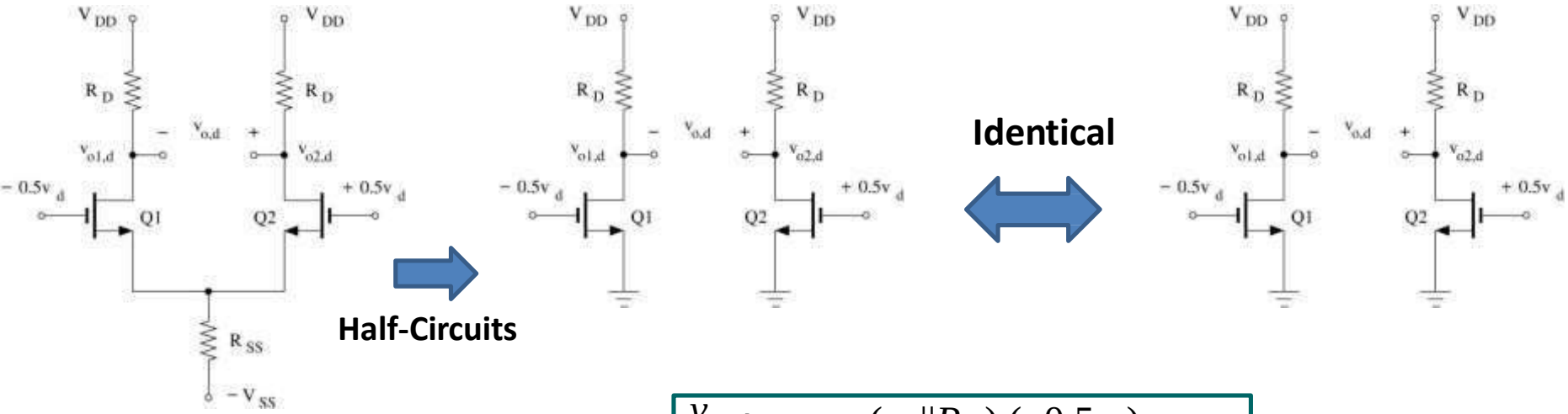
Two CS Amplifiers



Comparison of a differential amplifier with two identical CS amplifiers – Differential Mode

Differential amplifier

Two CS amplifiers



$$v_{o1,d} = -g_m (r_o \,||R_D)\,(-0.5v_d)$$

$$v_{o2,d} = -g_m (r_o \,||R_D)\,(+0.5v_d)$$

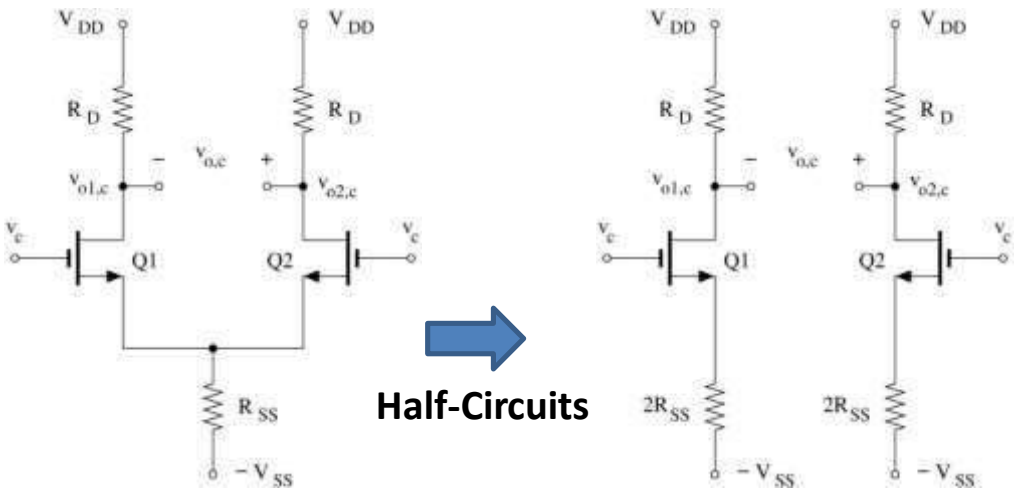
$$v_{od} = v_{o\,2,d} - v_{o1,d} = -g_m (r_o \,||R_D)\, v_d$$

$$A_d = v_{od} / v_d = -g_m (r_o \,||R_D)$$

- $v_{o1,d}$, $v_{o2,d}$, v_{od}, and differential gain, A_d, are identical.

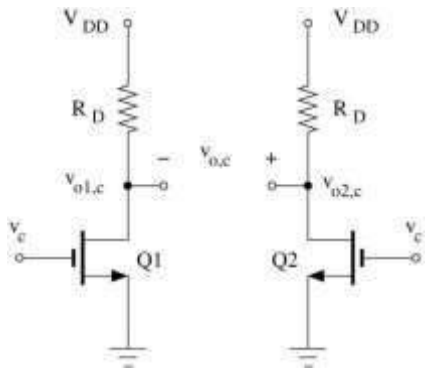
Comparison of a differential amplifier with two identical CS amplifiers – Common Mode

Differential amplifier



NOT Identical

Two CS amplifiers



$$v_{o1,c} = v_{o\,2,c} = -\frac{g_m R_D}{1 + 2g_m R_{SS} + R_D / r_o} v_c$$

$$v_{oc} = v_{o\,2,c} - v_{o1,c} = 0$$

$$A_c = v_{oc} / v_c = 0$$

$$v_{o1,c} = v_{o\,2,c} = -g_m (r_o \| R_D) v_c$$

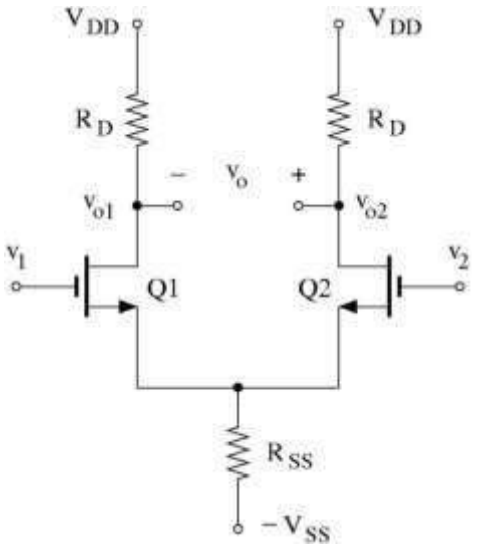
$$v_{oc} = v_{o\,2,c} - v_{o1,c} = 0$$

$$A_c = v_{oc} / v_c = 0$$

- $v_{o1,c}$ & $v_{o2,c}$ are different! But $v_{oc} = 0$ and CMMR = ∞.

Comparison of a differential amplifier with two identical CS amplifiers - Summary

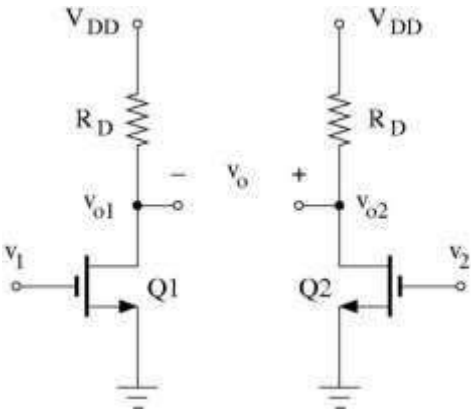
Differential Amplifier



$$A_d = \frac{v_{od}}{v_d} = -g_m\,(r_o \| R_D)\,,\; A_c = \frac{v_{oc}}{v_c} = 0$$

$$\text{CMRR} = \infty$$

Two CS Amplifiers



$$A_d = \frac{v_{od}}{v_d} = -g_m\,(r_o \| R_D)\,,\; A_c = \frac{v_{oc}}{v_c} = 0$$

$$\text{CMRR} = \infty$$

- **For perfectly matched circuits, there is no difference between a differential amplifier and two identical CS amplifiers.**
  - **But one can never make <u>perfectly</u> matched circuits!**

Configurations of Differential Amplifier:

- The differential amplifier in the difference amplifier stage in the op-amp, can be used in four configurations.

(i) Dual input, balanced output differential amplifier

(ii) Dual input, unbalanced output differential amplifier

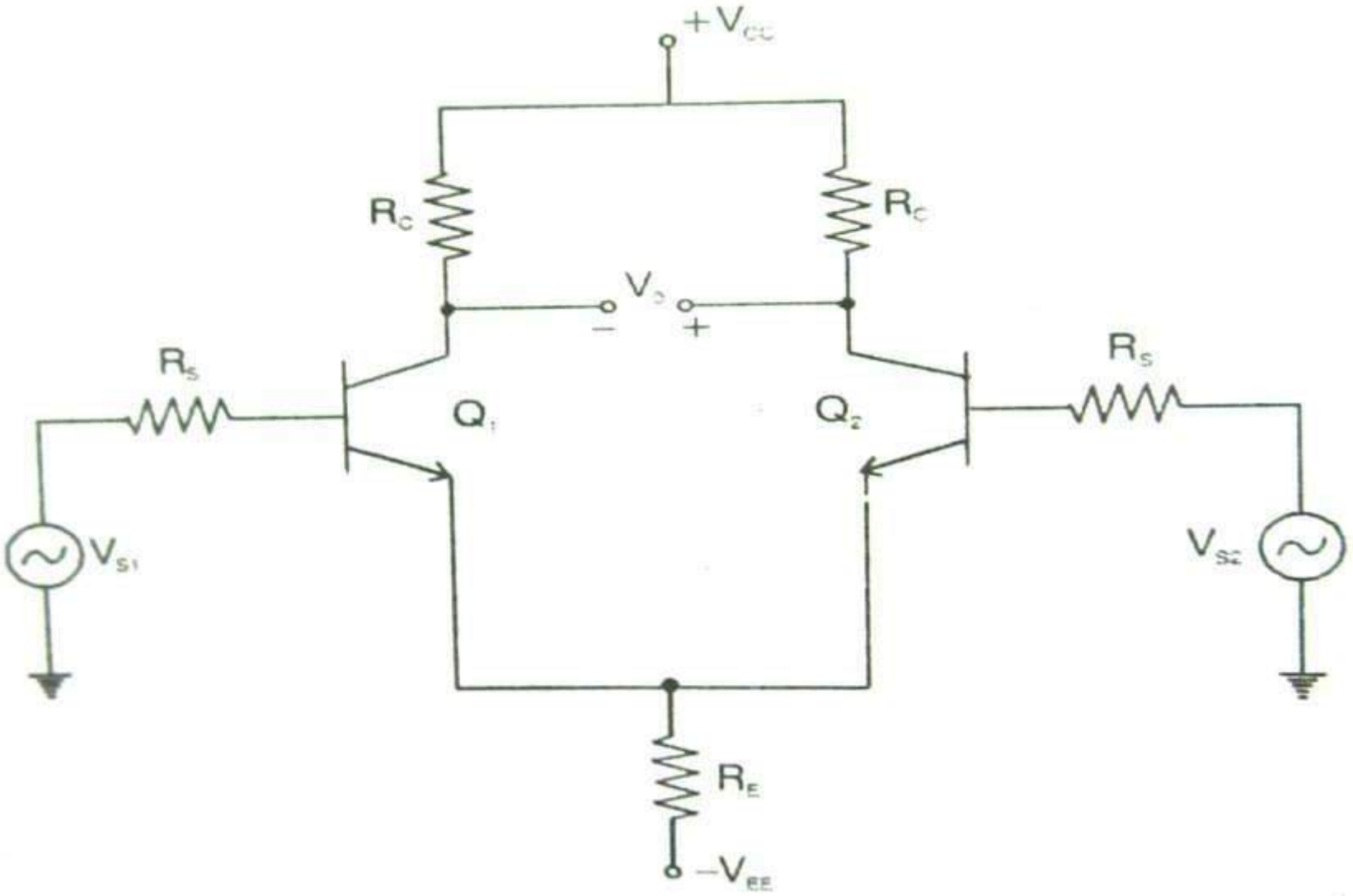
(iii) Single input, balanced output differential amplifier

(iv) Single input, unbalanced output differential amplifier

→ Out of these four configurations, the dual input, balanced output is the basic differential amplifier configuration.

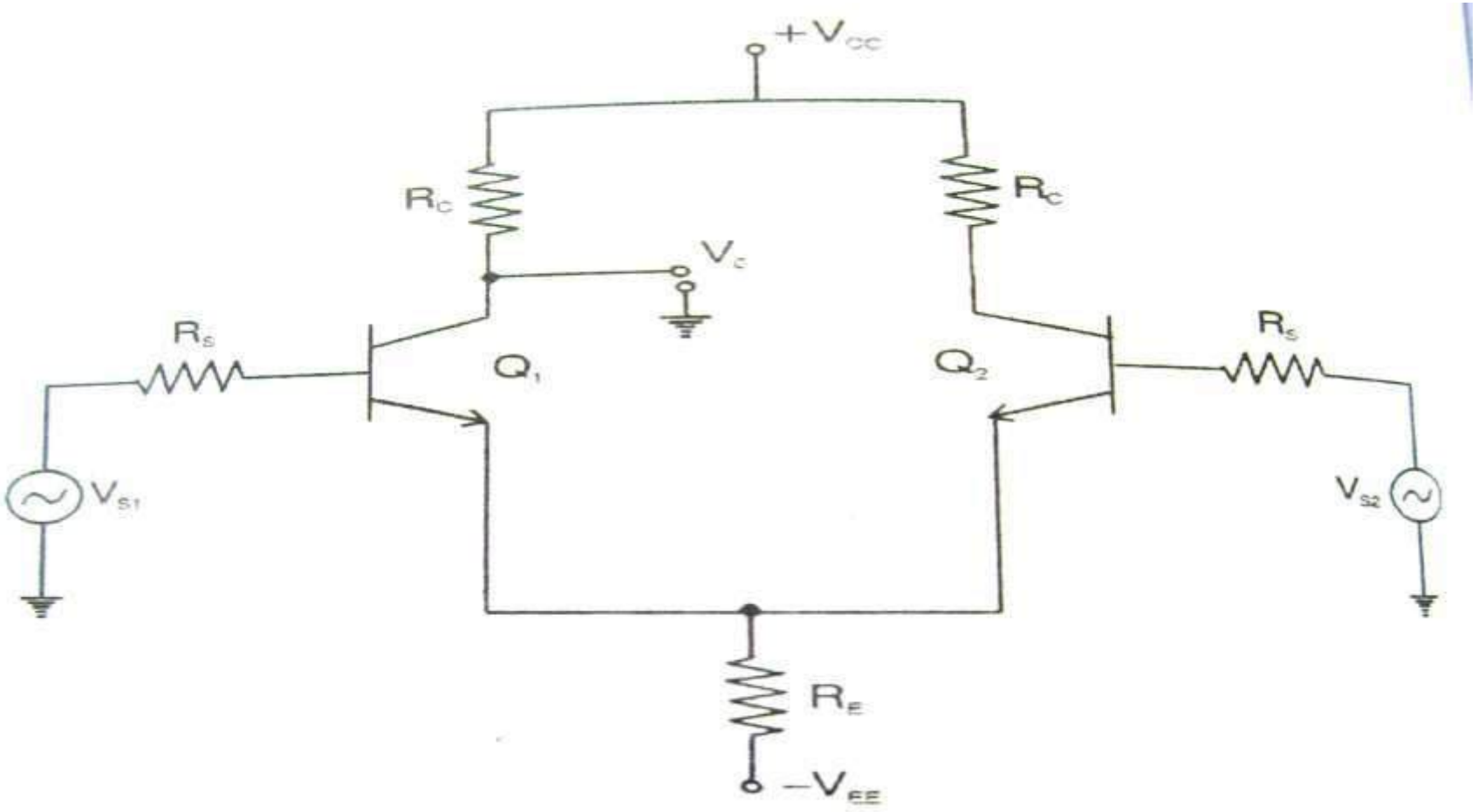
Dual input balanced output

differential amplifier



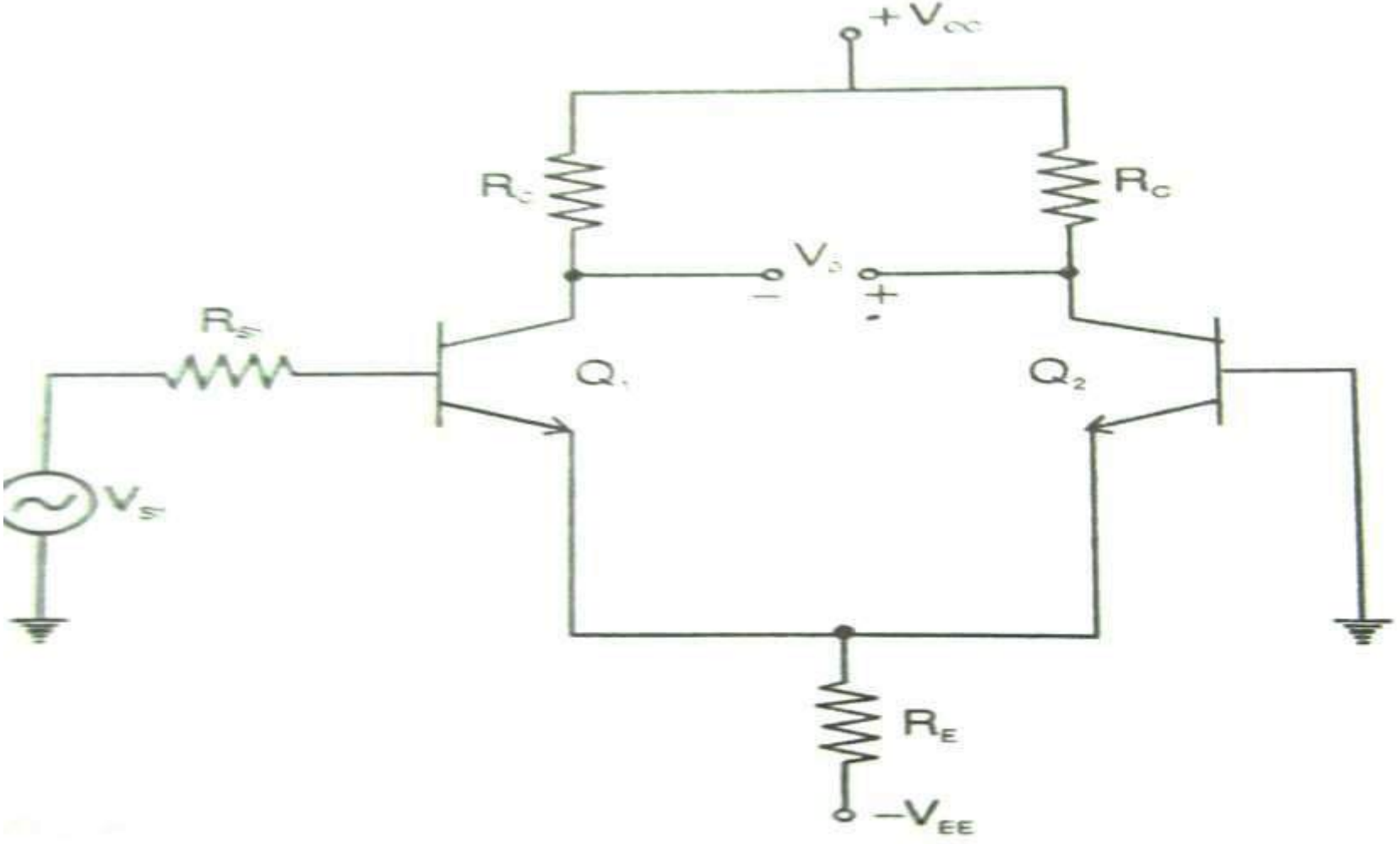
Dual input unbalanced output

differential amplifier



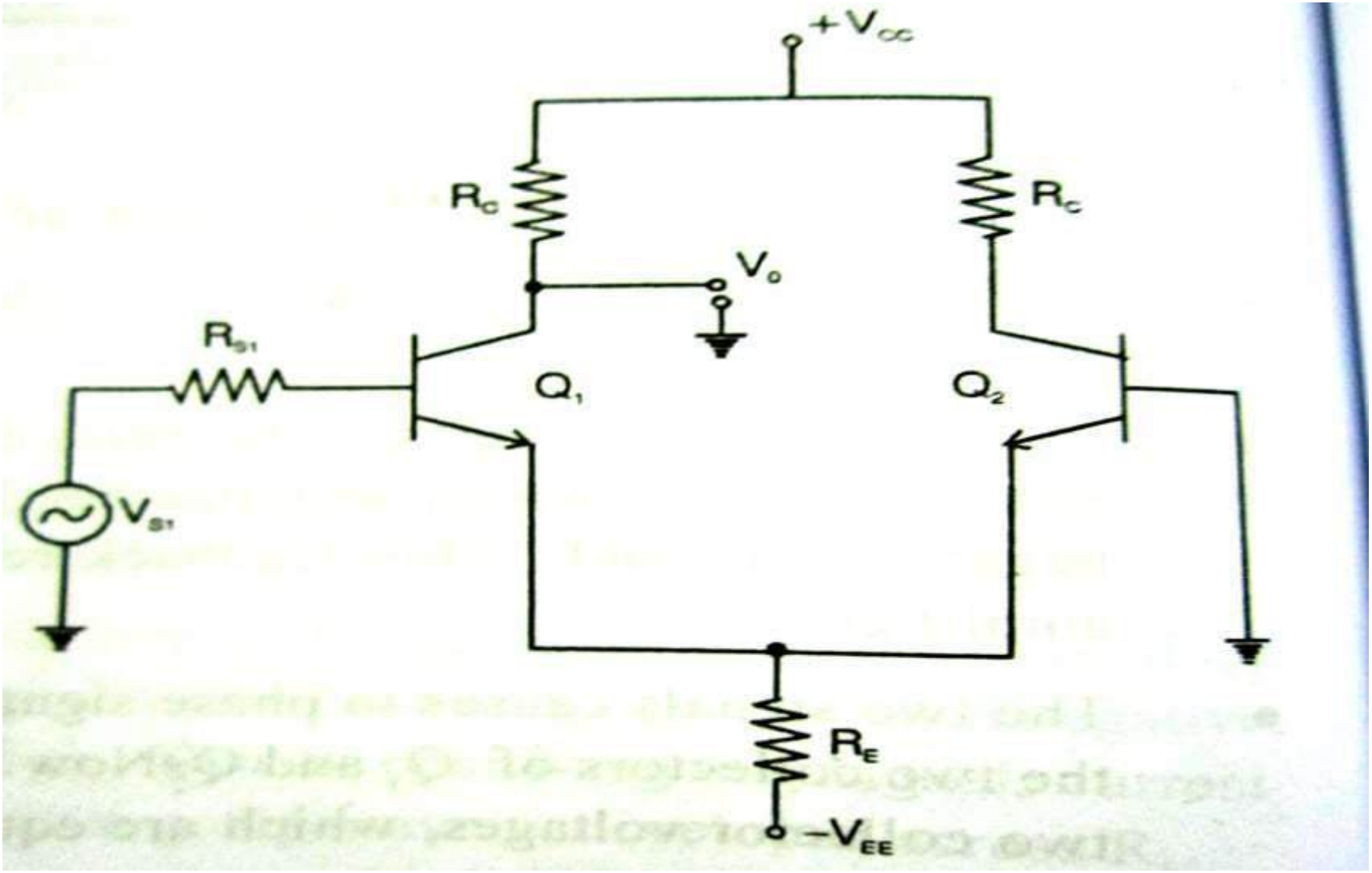
Single input balanced output

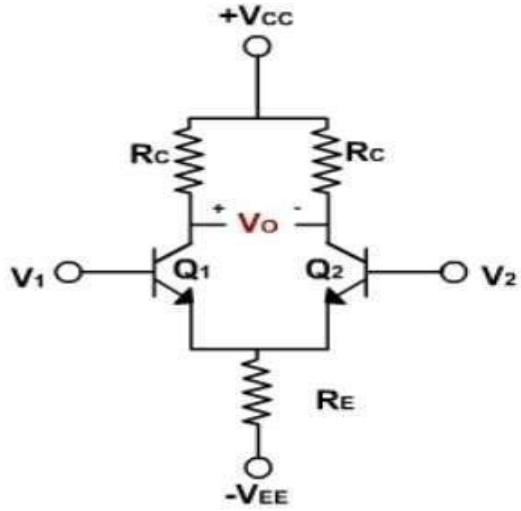
differential amplifier

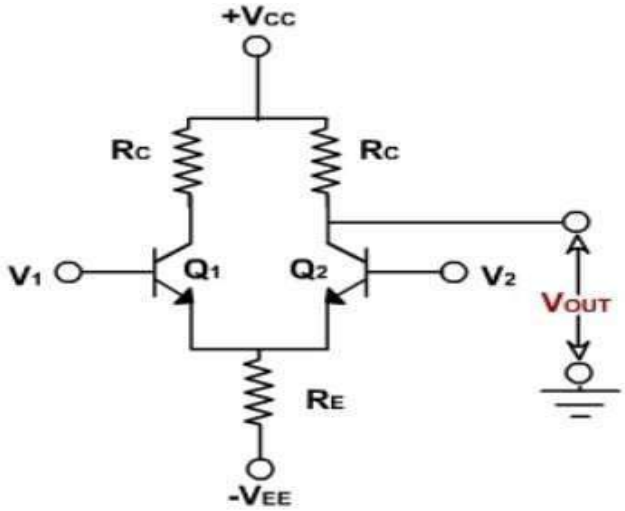


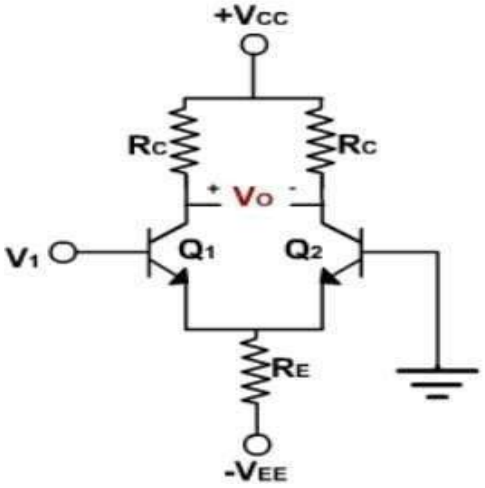
Single input unbalanced output

differential amplifier




+VCC
RC
RC
+
VO
-
V1
Q1
Q2
V2
RE
-VEE


+VCC
RC
RC
V1
Q1
Q2
V2
VOUT
RE
-VEE


+VCC
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RC
+
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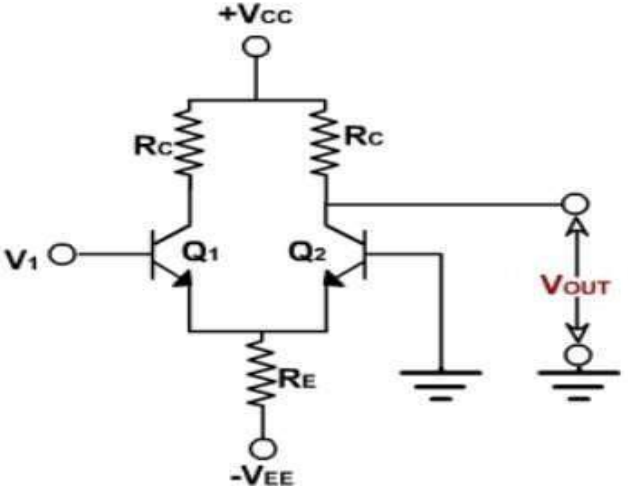
V1
Q1
Q2
RE
-VEE


+VCC
RC
RC
V1
Q1
Q2
VOUT
RE
-VEE

What is a current mirror?

It is a circuit that outputs a constant current that is equal to another current called “reference current”.

Q1 along with the series resistance determines the reference current.

While Q2 is responsible of delivering the output current or mirrored current to the load.

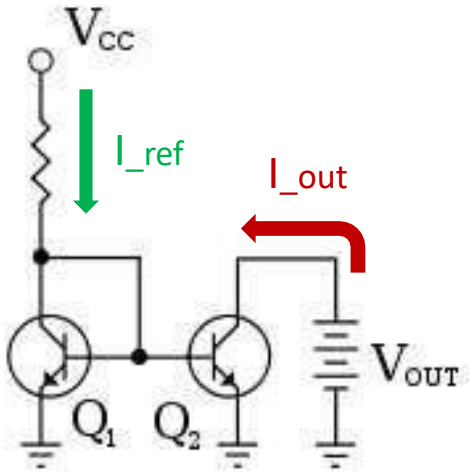
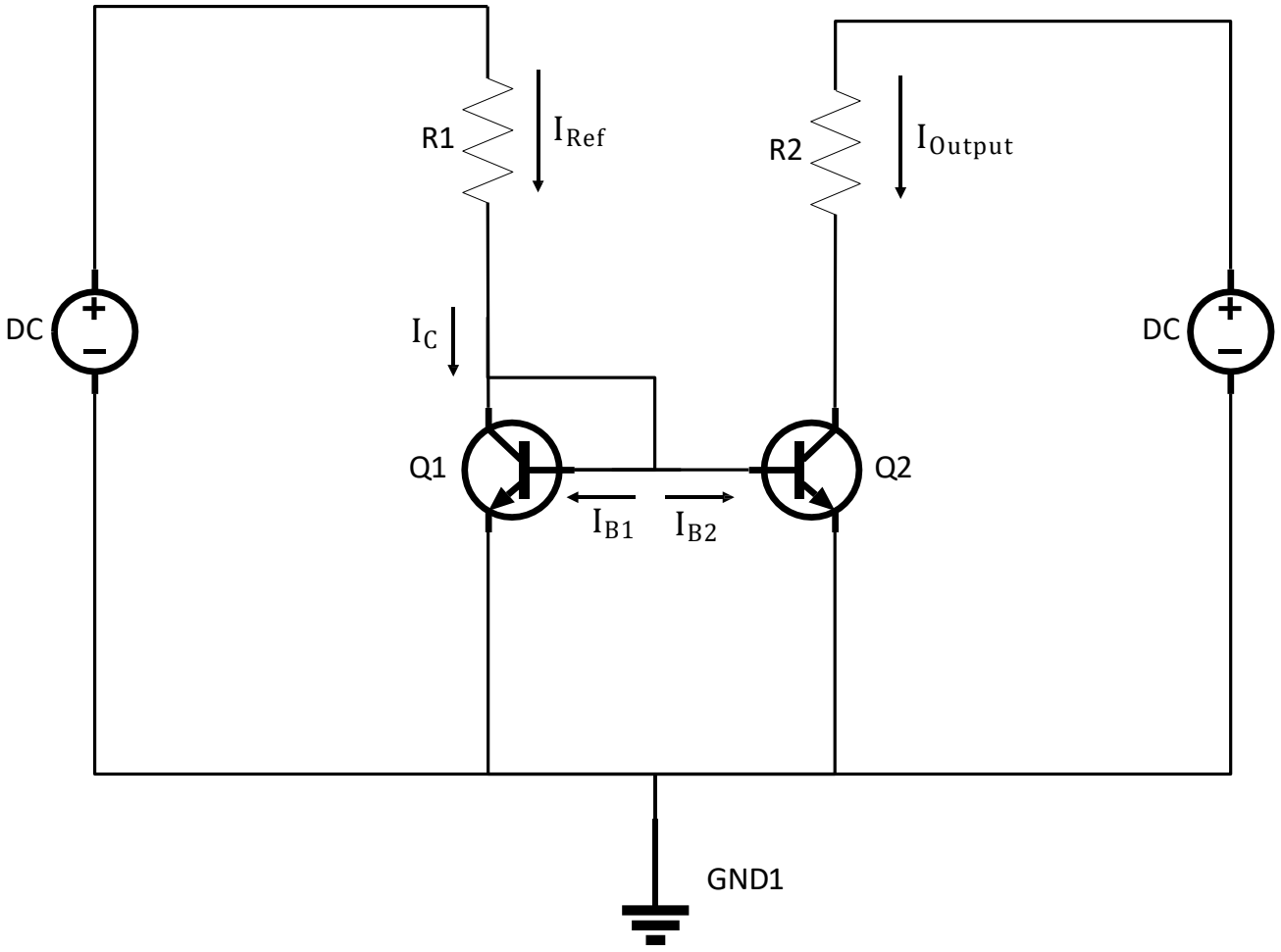


Figure 1: Current mirror basic circuit



Collector current is given by this equation:

$$I_C = \beta * I_B$$

Since the two transistors are identical:

$$I_{Ref} = I_C + 2\ I_B$$

Thus makes the output current:

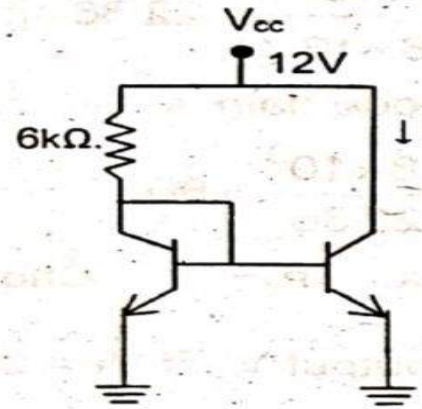
$$I_{\text{Output}} = I_C$$

Since base current is small compared to collector current, we can assume:

$$I_{\text{Output}} \approx I_{\text{Ref}}$$

GATE Questions with Solutions

1. A constant current source using two matched npn transistors with $\beta = 100$ and $V_{BE} = 0.6V$ is shown.
Calculate I_{out}



(A) 1.5mA (B) 0.2mA
(C) 1.86mA (D) 2mA

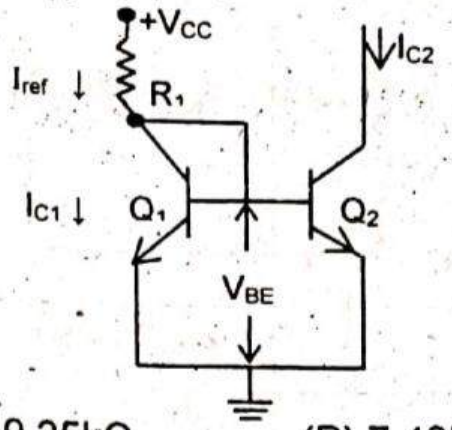
Sol. $I_{ref} = \dfrac{V_{CC} - V_{BE}}{R}$

$I_{ref} = \dfrac{12 - 0.6}{6K} = \dfrac{11.4}{6K} = 1.9mA$

$I_{OUT} = \dfrac{\beta}{2+\beta} I_{ref}$

$= \dfrac{100}{102} \times 1.9mA = 1.86mA$ Choice (C)

2. A current mirror shown below, provide a 1.5mA current with V_{CC} = 12V. Assume β = 150 and V_{BE} = 0.7volts. What is R_1.



(A) 9.25kΩ (B) 7.43kΩ
(C) 7.53kΩ (D) 8.5kΩ

Sol. $I_{C1} = I_{C2} = I_C$

$$I_C = \frac{\beta}{\beta+2} I_{ref}$$

$$\Rightarrow I_C = \left(\frac{\beta}{\beta+2}\right) \times \frac{(V_{CC} - V_{BE})}{R_1}$$

$$\Rightarrow 1.5\times10^{-3} = \frac{150}{152} \times \frac{(12-0.7)}{R_1}$$

$$R_1 = \frac{11.15}{1.5} K\Omega = 7.43K\Omega$$

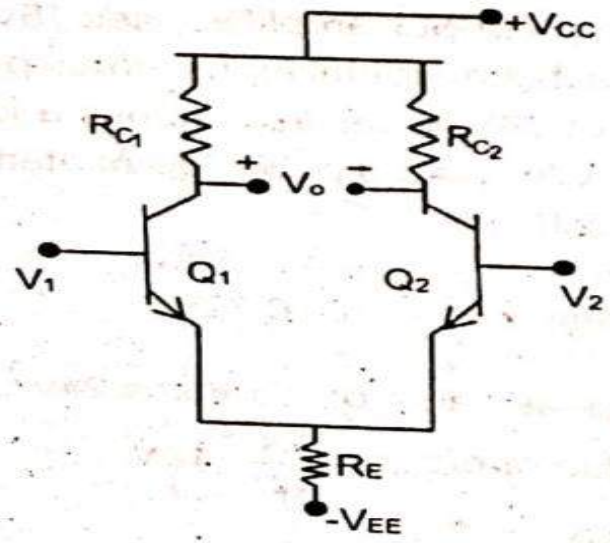
Choice (B)

Common Data for Questions 5 to 7:

A differential amplifier is shown below, has following specifications.

$R_{C_1} = R_{C_2} = 1.8K\Omega, R_E = 4K\Omega, V_{CC} = 10V, -V_{EE} = -10V$

$\beta = 100$ and $V_{BE} = 0.7\ V$



5. The emitter current I_E is

(A) 2.3mA (B) 1.16mA

(C) 1.7mA (D) 0.98mA

Sol. $2I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{10 - 0.7}{4K}$

$\Rightarrow I_E = \dfrac{9.3}{8}\text{mA} = 1.16\text{mA}.$ Choice (B)

6. The differential mode voltage gain A_d is

(A) 10 (B) 8 (C) 80 (D) 40

Sol. ac emitter resistance is

$$r_e = \frac{V_T}{I_E} = \frac{26\times10^{-3}}{1.16\times10^{-3}} = 22.36$$

differential mode gain is

$$A_d = \frac{R_C}{r_e} = \frac{1.8\times10^3}{2236} = 80$$

(Where $R_{C_1} = R_{C_2} = R_C$) Choice (C)

7. What is the output V_O if $V_1 = 30mV$ and $V_2 = 40mV$

(A) 0.8V (B) 5.6V (C) 2.8V (D) 0V

8/16

Sol. $A_d = \frac{V_o}{V_{id}}$

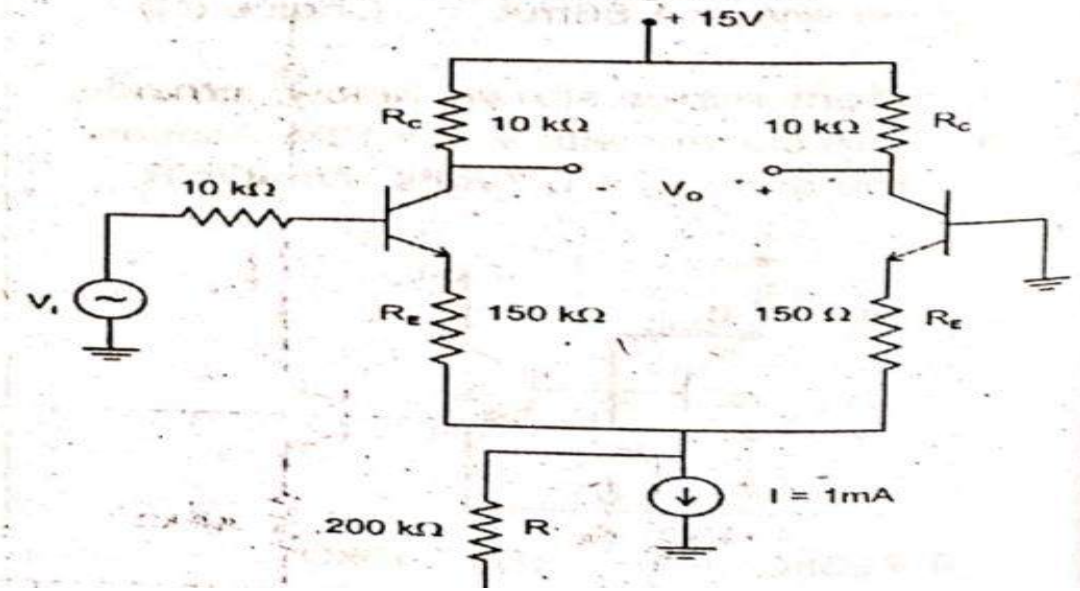
$V_O = A_d V_{id} = A_d(V_2 - V_1)$

$= 80(40 - 30)mV$

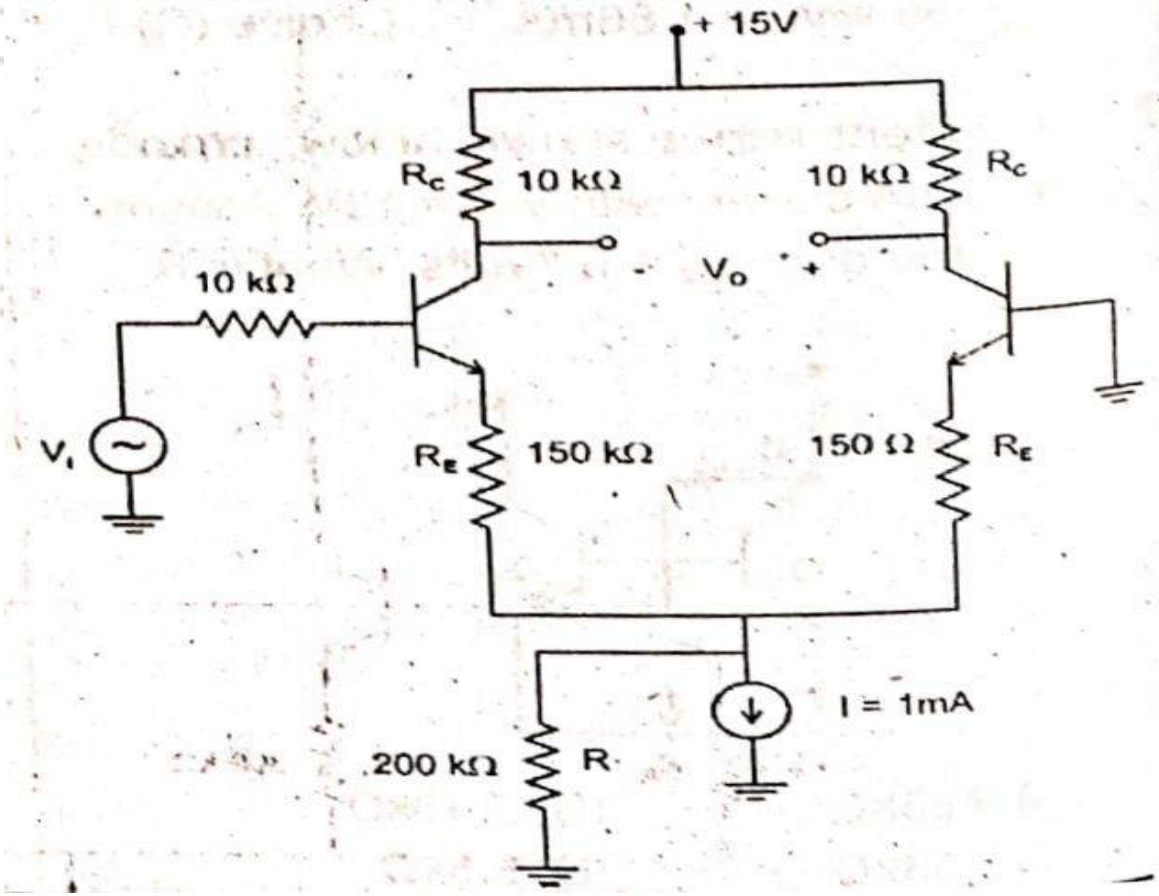
$= 800mV$

$= 0.8V$ Choice (A)

8. Consider the following circuit



8. Consider the following circuit



The tansistors have $\beta = 100$. Determine the input differential resistance R_{id}, overall voltage gain $\frac{V_o}{V_i}$ and the worst case common mode rejection ratio if two collector resistances are accurate within ± 1 %

Sol. Each transistor is biased at an emitter current of 0.5 mA in case of symmetric feed, here feed is not symmetric but results will be similar in both cases.

$$\therefore r_{e1} = r_{e2} = \frac{V_T}{I_E} = \frac{25\text{ mV}}{0.5\text{ mA}} = 50\ \Omega$$

∴ Input differential resistance can now be find as

$Rid = 2(\beta + 1)(r_e + R_E)$

Where $\beta = 100$

$R_E = 150\ \Omega$

$\therefore R_{id} = 2(100 + 1)(50 + 150)$

$R_{id} = 40{,}400\ \Omega$

$R_{id} = 40.4\ K\Omega$

Given $R_s = 10\ K\Omega$

Voltage gain from the signal source to base Q1 and Q2 is

$$\frac{V_{id}}{V_i} = \frac{R_{id}}{R_{id} + R_s} = \frac{40.4}{40.4 + 10} \cong 0.80$$

$$\frac{V_o}{V_{id}} = \frac{2R_C}{2(r_e + R_E)}$$

$$= \frac{2 \times 10}{2(50 + 150) \times 10^{-3}}$$

$$\frac{V_o}{V_{id}} = 50$$

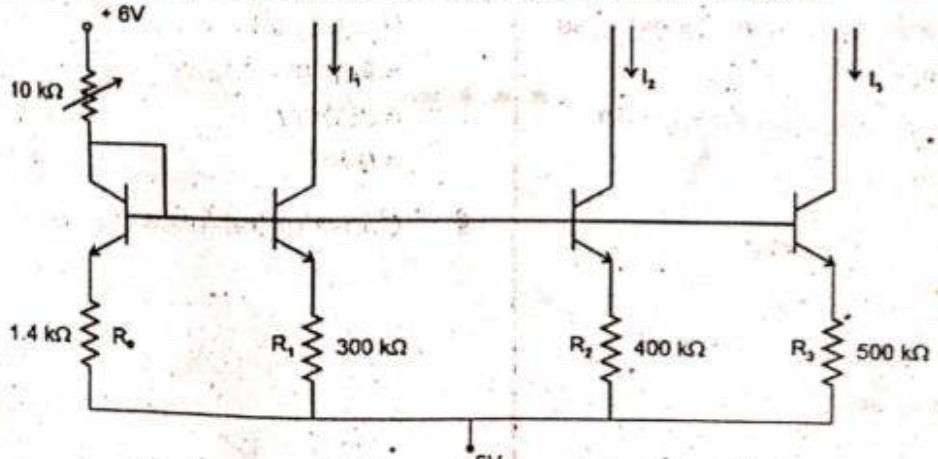
$$A_d = \frac{V_o}{V_i} = \frac{V_o}{V_{id}} \times \frac{V_{id}}{V_i}$$

$$\frac{V_o}{V_{id}} = 50 \times 0.8 = 40$$

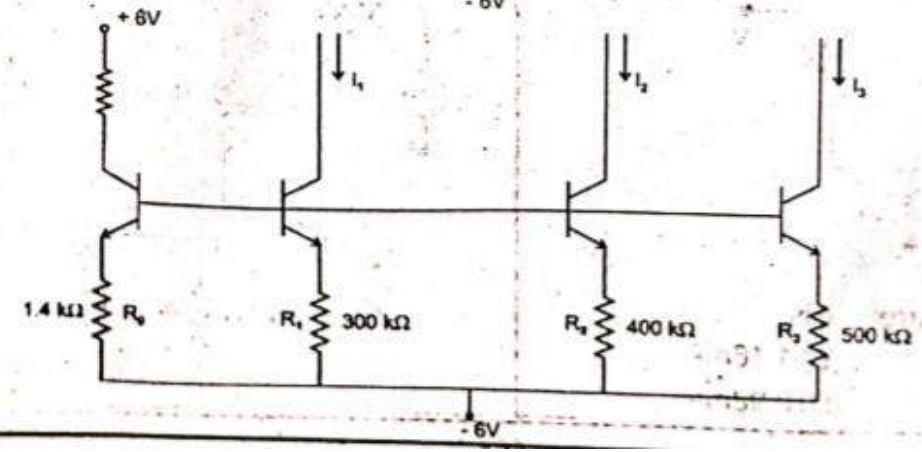
$$A_{cm} = \frac{R_C}{2R_{EE}} \frac{\Delta R_C}{R_C} = 5 \times 10^{-4}$$

$$C_{MRR} = 20 \log \frac{A_d}{A_{CM}} = 98.06\text{ dB}.$$

9. For the circuit shown, neglecting base currents, find I_0 and I_1, I_2, I_3.



Sol.



The base currents are neglected i.e β of the transistors are very high.

Applying KVL in 1st transistor

$6 - I_o (10\ K) - 0.7 - 1.4\ KI_o + 6 = 0.$

$11.3 = I_o (10 + 1.4)\ K$

$I_o = \frac{11.3}{11.4}\ mA$

$I_o \simeq 1\ mA$

Since all transistors are coupled to each other, therefore emitter voltages are same in all the transistors as they are connected in parallel.

$\therefore V_{R_O} = 1.4\ K \times 1\ mA = 1.4\ V$

$V_{R1} = 1.4\ V = I_1 \times 300$

$I_1 = \frac{1.4}{300} = 4.67\ mA$

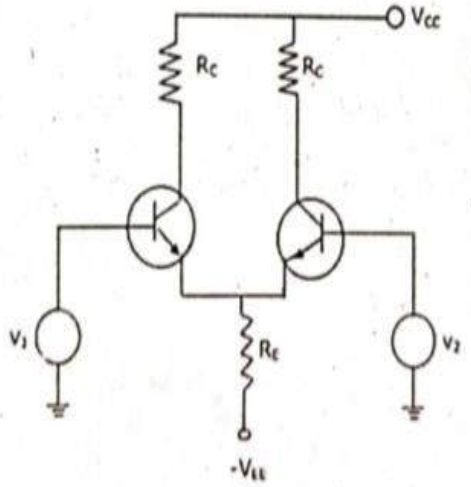
$V_{R2} = 1.4\ V = I_2 \times 400$

$I_2 = \frac{1.4}{300} = 3.5\ mA$

$V_{R3} = 1.4\ V = I_2 \times 500$

$I_2 = \frac{1.4}{500} = 2.8\ mA.$

In an ideal differential amplifier shown in figure, a large value of R_E



(A) increase both the differential and common - mode gains.
(B) increase the common-mode gain only
(C) decreases the differential-mode gain only
(D) decreases the common -mode gain only.

2. In ideal differential amplifier

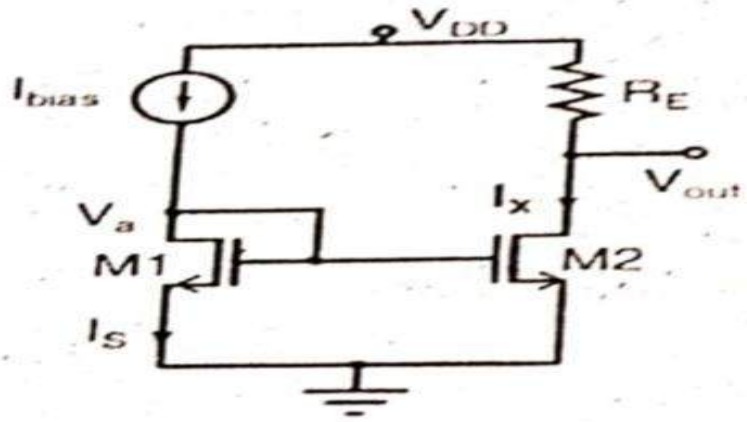
Differential mode Gain = $-g_m R_c$

Common mode gain = $\frac{-R_C}{2R_E}$

By increasing emitter resistance value, common mode gain will be decreased and differential mode gain does not vary.

Choice (D)

3. For the circuit shown in the following figure, transistors M1 and M2 are identical NMOS transistors. Assume that M2 is in saturation and the output is unloaded



(GATE 2008)

The current I_x is related to I_{bias} as

(A) $I_x = I_{bias} + I_s$

(B) $I_x = I_{bias}$

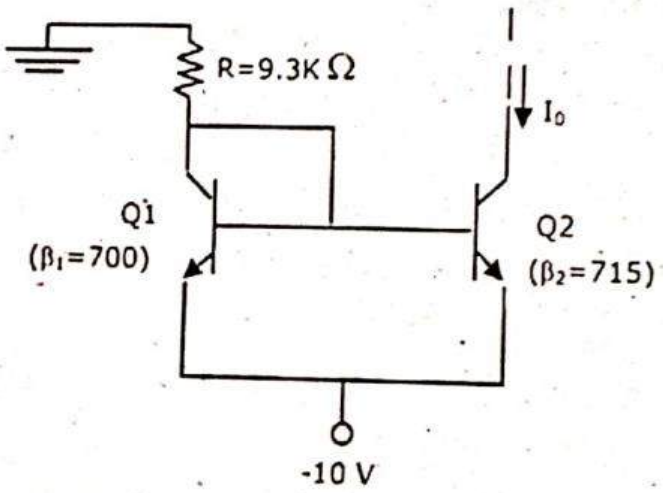
(C) $I_x = I_{bias} - I_s$

(D) $I_x = I_{bias} - \left(V_{DD} - \frac{V_{out}}{R_E} \right)$

Given circuit is current mirror circuit is equally divided , Ibias = Ix

Choice : B

4. In the silicon BJT circuit shown below, assume that the emitter area of transistor Q_1 is half that of transistor Q_2.



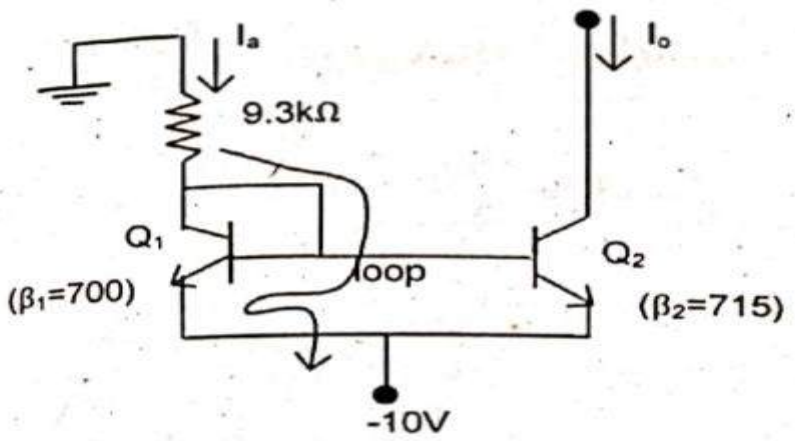
The value of current I_0 is approximately

(GATE 2010)

(A) 0.5 mA (B) 2mA

(C) 9.3 mA (D) 15mA

4.



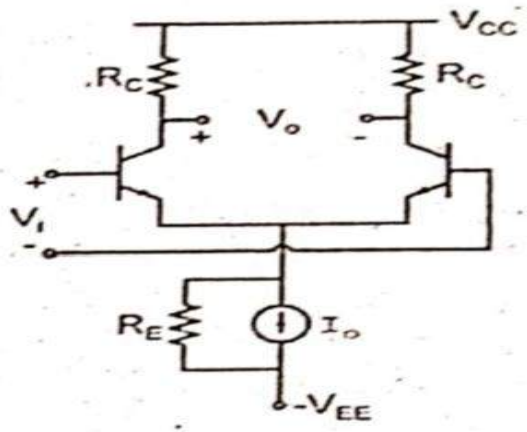
$$I_a = \frac{10-0.7}{9.3\times10^3} = 1mA$$

$$\frac{I_o}{I_a} = \frac{\text{area of } Q_2 \text{ transistor}}{\text{area of } Q_1 \text{ transistor}}$$

Given that $A_{Q_1} = \frac{A_{Q_2}}{2} \Rightarrow I_o = 2Ma.$

Choice (B)

5. In the differential amplifier shown in the figure, the magnitudes of the common-mode and differential-mode gains are A_{cm} and A_d, respectively. If the resistance R_E is increased, then

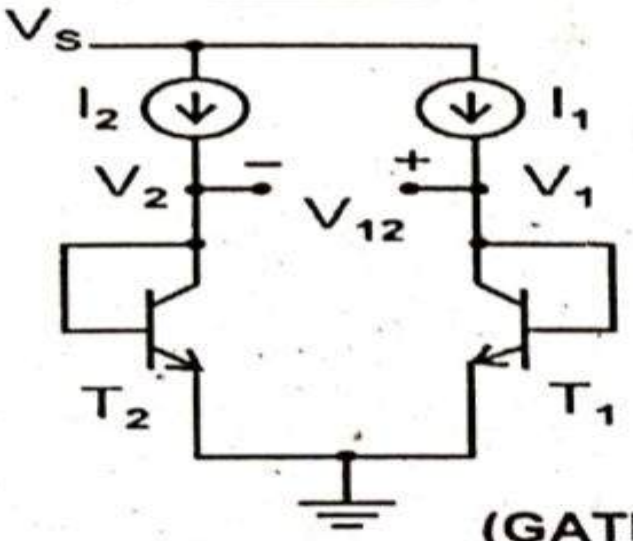


(GATE 2014, Set-2)

(A) A_{cm} increases
(B) common-mode rejection ratio increases
(C) A_d increases
(D) common-mode rejection ratio decreases

Choice : B
If the resistance Re increases ,then the CMRR gain improved because common mode gain is small

7. In the circuit shown, I_1 = 80 mA and I_2 = 4 mA. Transistors T_1 and T_2 are identical. Assume that the thermal voltage V_T is 26 mV at 27°C. At 50°C, the value of the voltage $V_{12} = V_1 - V_2$ (in mV) is _____



(GATE 2015, Set-1)

7. From the given data

$I_1 = 80$ mA and $I_2 = 4$ mA

$V_T = 26$ mV at 27°C

At 50°C, the value of the voltage V_{12} $= V_1 - V_2 = ?$

We know

$$I = I_o \left\{e^{V/\eta V_T} - 1\right\},\ I \approx I_o \left\{e^{V/\eta V_T}\right\}$$

$$\frac{I_1}{I_2} = e^{(V_1 - V_2)/\eta \cdot V_T}$$

We know $V_T = \dfrac{T}{11600}$

at $T = 273 + 50° = 323°$ K

$$V_T = \frac{323}{11600} = 27.844\ \text{mV}$$

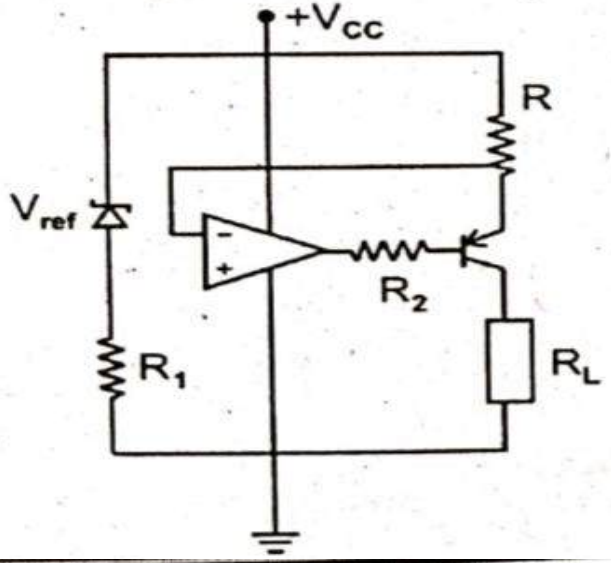
$$V_{12} = \eta V_T . \ln\left(\frac{I_1}{I_2}\right) \text{V}$$

Let $\eta = 1$ (NOT given)

$$V_{12} = 27.844 \times 10^{-3} . \ln\left(\frac{80}{4}\right)$$

$= 83.413$ mV Ans: 83.5 to 84.0

8. Consider the constant current shown in the figure below. Let β represent the current gain of the transistor



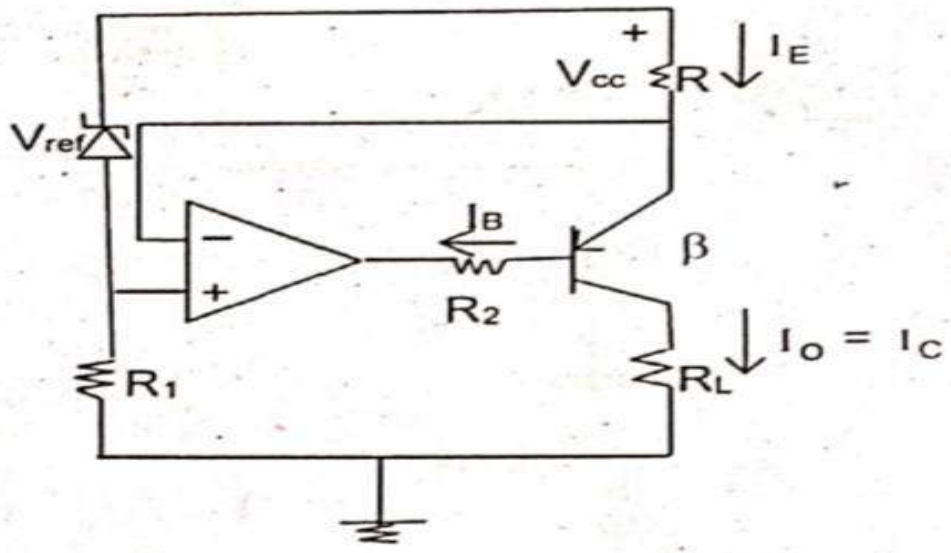
The load current I_o through R_L is

(GATE 2016, Set-1)

(A) $I_o = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{R}$ (B) $I_o = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{R}$

(C) $I_o = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{2R}$ (D) $I_o = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{2R}$

8. Re draw the given circuit



$$I_E = I_B + I_C = (1+\beta) I_B$$

$$\frac{V_{ref}}{R} = (1+\beta) I_B$$

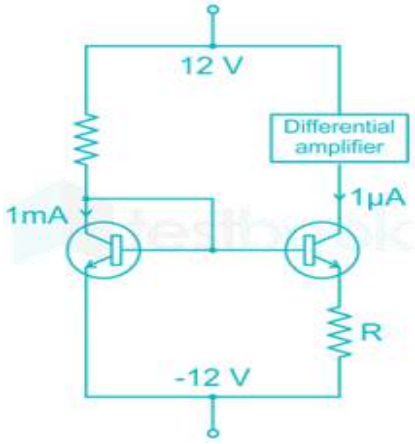
$$I_C = \beta . I_B$$

$$I_B = \frac{I_C}{\beta}$$

$$\therefore I_C = I_O = \left(\frac{\beta}{1+\beta}\right) \frac{V_{ref}}{R}$$

Choice (B)

5. The circuit shown in the figure uses matched transistors with a thermal voltage V_T = 25 mV. The base currents of the transistors are negligible. The value of the resistance R in kΩ that is required to provide 1 μA bias current for the differential amplifier block shown is ___. (Give the answer up to one decimal place.)



Given that, I_{cl} = 1 mA, I_{c2} = 1 μA

V_T = 25 mV

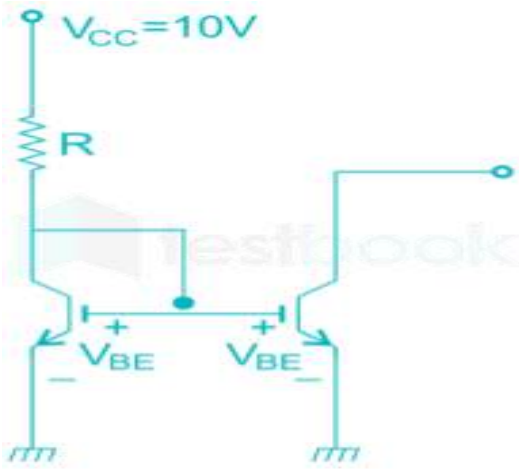
$I_{B1} = I_{B2} = 0$

$$R = \frac{V_T}{I_{c2}} \ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

$$= \frac{25 \times 16^3}{10^{-6}} \ln\left(\frac{10^{-3}}{10^{-6}}\right)$$

$$= \frac{25}{10^{-3}} \ln(1000) = 172.7 k\Omega$$

54. The current mirror of figure is designed to provide I_C = 0.5 mA. V_{CC} = 10 V, β = 125. The value of R is ____ kΩ



Output current I_C =0.5 mA

Therefore base current $I_B = \frac{I_C}{\beta} = \frac{0.5\text{ mA}}{125} = 4\ \mu A$

Now the current through resistor R is.

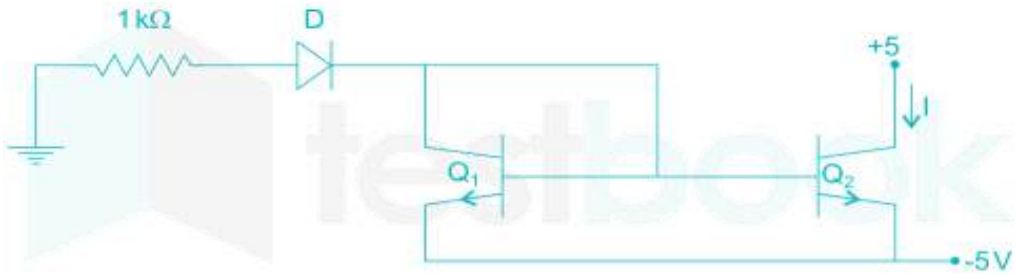
$I_R = I_C + I_B$ =0.5 mA+8 μA =0.508 mA

$V_{BE} \simeq 0.7V$

Therefore voltage drop across R is 10V–0.7V=9.3V

$\therefore R = \frac{9.3}{0.508} = 18.307\ k\Omega$

37. Two perfectly matched silicon transistor are connected as shown in the figure. Assuming the β of the transistor to be very high and forward voltage drop to be 0.7 V, V_{BE} = 0.7, the value of current I is



1. 0 mA **2. 3.6 mA** **3. 4.3 mA** **4. 5.7 mA**

This is a current mirror circuit, since β is very large,

$I_{C_1} = I_{C_2} = I_C = I_{E_1} = I_{E_2} = I_E$ and $I_{B_1} = I_{B_2} = I_B = 0$

Apply KVL through Q1 from -5V to ground.

Ix1K + 0.7 + 0.7 = 5

∴ D is forward biased.

Current passing through diode is

$I = \frac{3.6}{1k} = 3.6\ mA$