Buses

The primary function of the bus is to provide a communication path for the transfer of data. It must also look in to

* when to place information on the bus?
* when to have control signals?

Some bus protocols are set. These involve data, address and control lines. A variety of schemes have been devised, for the timing of data transfers over a buses They are;

* Synchronous
* Asynchronous schemes

Synchronous Bus: All devices derive timing information from a common clock line. Equally spaced pulses on this line define equal time intervals. Each of these intervals constitutes a bus cycle during which one data transfer can take place.

Asynchronous Bus: This is a scheme based on the use of a hand shake between the master and the slave for controlling data transfer on the bus.

The common clock is replaced by two timing control lines, master-ready and slave-ready. The first is asserted by the master to indicate that it is ready for a transaction and the second is a response from the slave. The master places the address and command information on the bus. It indicates to all devices that it has done so by activating the master-ready line. This causes all devices on the bus to decode the address. The selected slave performs the required operation and informs the processor it has done so by activating the slave-ready line. A typical hand shake control of data transfer during an input and an output operation. A change of state in one signal is followed by a change in the other signal. Hense this scheme is known as a full handshake.