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SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME : 23EET206 CONTROL SYSTEMS AND INSTRUMENTATION

II YEAR ECE /III SEMESTER

Unit 5-Oscilloscope, Signal Generator, Analyzer and Data Acquisition System

Topic 3 : Frequency Synthesized Signal Generator

FREQUENCY SYNTHESIZER

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- A **frequency synthesizer** is an electronic circuit that generates a range of frequencies from a single reference frequency.
- Frequency synthesizers are used in devices such as radio receivers, televisions, mobile telephones, radiotelephones, walkie-talkies, CB radios, cable television converter boxes, satellite receivers, and GPS systems.
- A frequency synthesizer may use the techniques of frequency multiplication, frequency division, direct digital synthesis, frequency mixing, and phase-locked loops to generate its frequencies. The stability and accuracy of the frequency synthesizer's output are related to the stability and accuracy of its reference frequency input.

FREQUENCY SYNTHESIZER

A **frequency synthesizer** can be of two types

- Direct Method (Direct Analog Synthesis or Direct Digital Synthesis)
- Indirect Method (Phase Locked Loop, Integer N Synthesizer and Fractional N Synthesizer)

PHASE LOCKED LOOP

- A Phase-Locked Loop (PLL) is a negative feedback system consists of a phase detector, a low pass filter and a voltage controlled oscillator (VCO) within its loop.
- Its purpose is to synchronize an output signal with a reference or input signal in frequency as well as in phase.
- In the synchronized or “locked” state, the phase error between the oscillator’s output signal and the reference signal is zero, or it remains constant.
- If a phase error builds up, a control mechanism acts on the oscillator to reduce the phase error to a minimum so that the phase of the output signal is actually locked to the phase of the reference signal. This is why it is called a PLL.

PHASE LOCKED LOOP

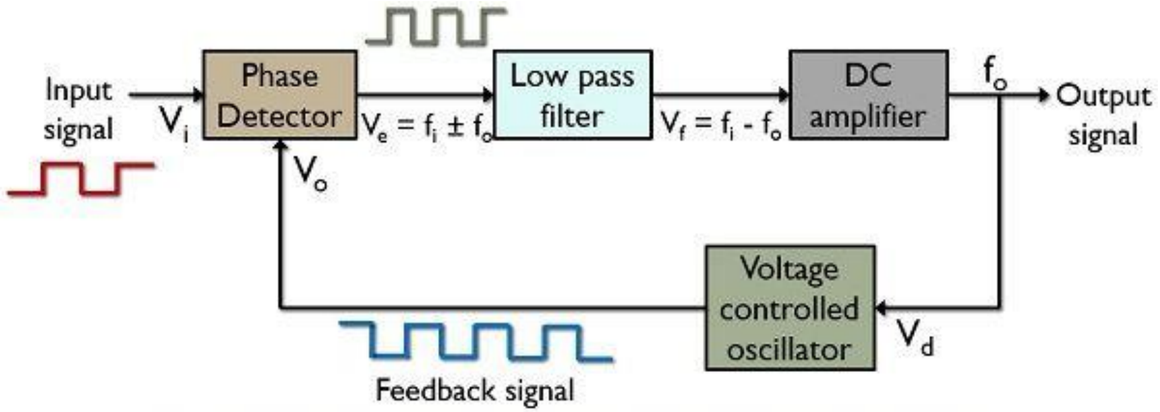
The majority of PLL applications fall into four main categories:

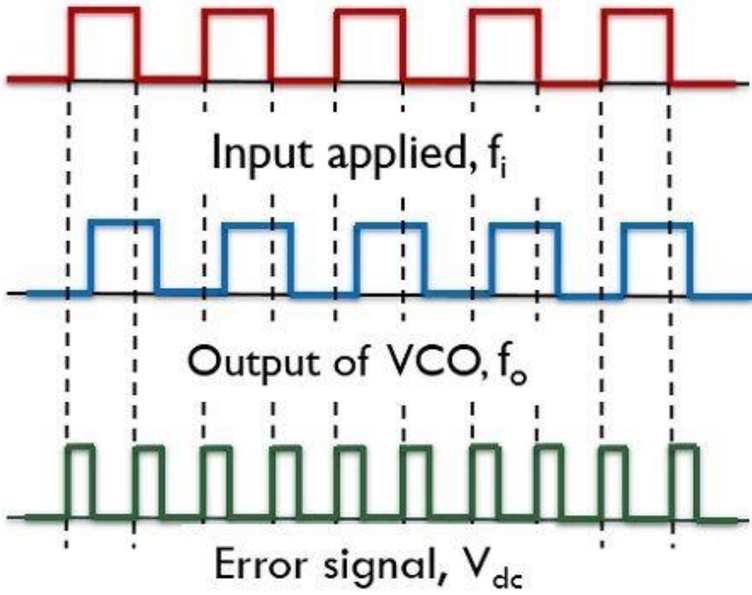
- Frequency synthesis
- Frequency (FM) and phase (PM) modulation and demodulation.
- Data and carrier recovery.
- Tracking filters.

Classification of PLLs:

- Analog or Linear PLL (LPLL), Digital PLL (DPLL) is Analog PLL with digital phase detector
- All-Digital PLL (ADPLL) is a digital loop in two senses: all digital components and all digital (discrete-time) signals.

PHASE LOCKED LOOP





The basic PLL block diagram consists of three components connected in a feedback loop :

- **A Phase Detector (PD)** or **Phase Frequency Detector (PFD)**
  - produces a signal $\mathbf{V_\phi}$ proportional to the phase difference between the $\mathbf{f_{in}}$ and $\mathbf{f_{osc}}$ signal.
- **A Loop Filter (LF)**
  - filters output voltage $\mathbf{V_{out}}$ that controls the frequency of the VCO.
- **A Voltage-Controlled Oscillator (VCO)**
  - $\mathbf{V_{out}}$ at the input of the VCO determines the frequency $\mathbf{f_{osc}}$ of the periodic signal $\mathbf{V_{osc}}$ at the output of the VCO

PHASE LOCKED LOOP

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A basic property of the PLL atemps to maintain the frequency lock $f_{osc} = f_{in}$ between V_{osc} and V_{in} even if the frequency f_{in} of the incoming signal varies in time.

Assume the PLL is in the locked condition, and the frequency f_{in} of the incoming signal increases slightly. The phase difference between the VCO signal and the incoming signal will begin to increase in time. As a result, the filtered output voltage V_{out} increases the VCO output frequency f_{osc} increases until it matches f_{in}, thus keeping the PLL in the locked condition.

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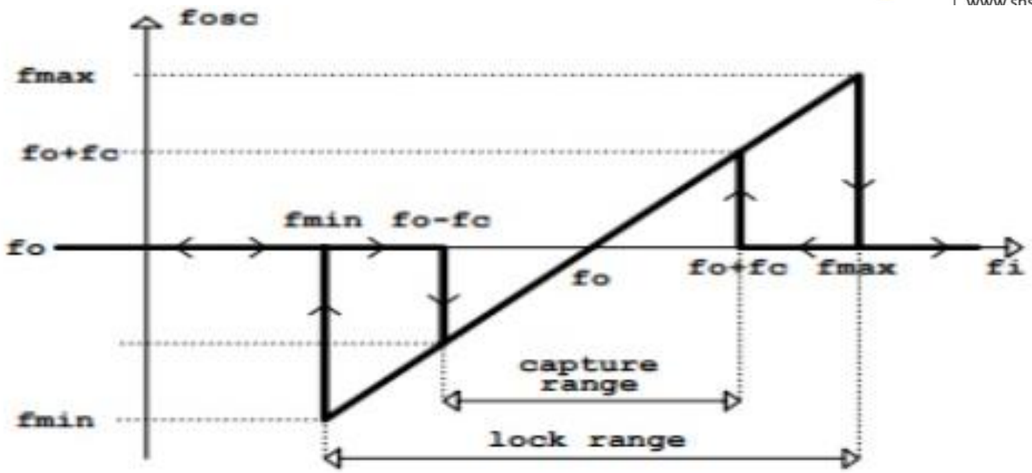
STAGES OF PLL

There are three stages of PLL operations:

- **Free Running Stage:** When no input is applied at the phase detector, PLL out put frequency is $f_{osc} = f_o$ where f_o free running frequency of the VCO.
- **Capture Stage:** When an input is applied at the phase detector and due to feedback mechanism PLL tries to track the output with respect to the input.
- **Phase Locked Stage:** Due to feedback mechanism, the frequency comparison stops when $f_{osc} = f_{in}$.



Lock Range and Capture Range of PLL:

Lock Range of the PLL: The range of frequencies where the locked PLL remains in the locked: $f_{min} \le f_{in} \le f_{max}$
The lock range is wider than the capture range.

- If the PLL is initially locked, and if $f_{max} < f_{in} < f_{min}$ the PLL becomes unlocked ($f_{in} \ne f_{osc}$).
- When the PLL is unlocked, the $f_{osc} = f_o$ where f_o is called the center frequency, or the free-running frequency of the VCO.

Capture Range of the PLL: The lock can be established again if the incoming signal frequency f_{in} gets close enough to f_o.
The range of frequencies such that the initially unlocked PLL becomes locked: $f_o - f_c \le f_{in} \le f_o + f_c$
Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

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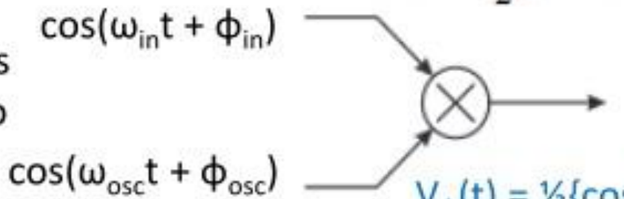
Linear (Analog) Phase Detector

$$\cos\alpha\cos\beta = \frac{1}{2}\left[\cos(\alpha-\beta)+\cos(\alpha+\beta)\right]$$



$V_\phi(t) = \frac{1}{2}\{\cos(\phi_{osc} - \phi_{in}) + \cos[(2\omega_{osc}t) + (\phi_{osc} + \phi_{in})]\}$

High frequency component to be removed by low-pass filter

An analog multiplier mixer can be used as a phase detector which compares the phase at each input and generates an error signal, $V_\phi(t)$, proportional to the phase difference between the two inputs.

Recall that the mixer takes the product of two inputs.

$V_\phi(t) = \cos(\omega_{osc}t + \phi_{osc})\ \cos(\omega_{in}t + \phi_{in})$

$= (1/2)\ \{\cos[(\omega_{osc}t - \omega_{in}t) + (\phi_{osc} - \phi_{in})] + \cos[(\omega_{osc}t + \omega_{in}t) + (\phi_{osc} + \phi_{in})]\}$

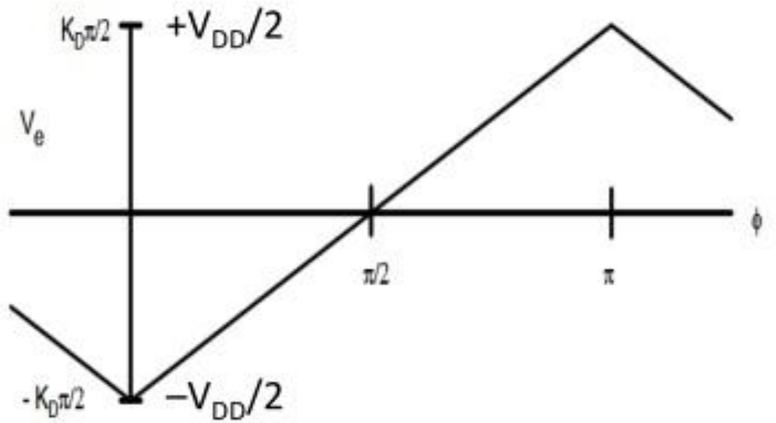
When loop is locked ($\omega_{osc} = \omega_{in}$) ⇒ we have an output proportional to the cosine of the phase difference and **one output at twice the input frequency** .

$V_\phi(t) = (1/2)\ \{\cos(\phi_{osc} - \phi_{in}) + \cos[(2\omega_{osc}t) + (\phi_{osc} + \phi_{in})]\}$

The doubled frequency component will be removed by the low-pass loop filter. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering. K_D is the gain of the phase detector (V/rad).

$V_\phi(t) = K_D\ (\phi_{osc} - \phi_{in})$ where $K_D\ \pi/2 = V_{DD}/2$ ⇒ **$K_D = V_{DD}/\pi$**

The averaged transfer characteristic of such a phase detector is shown below. Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).



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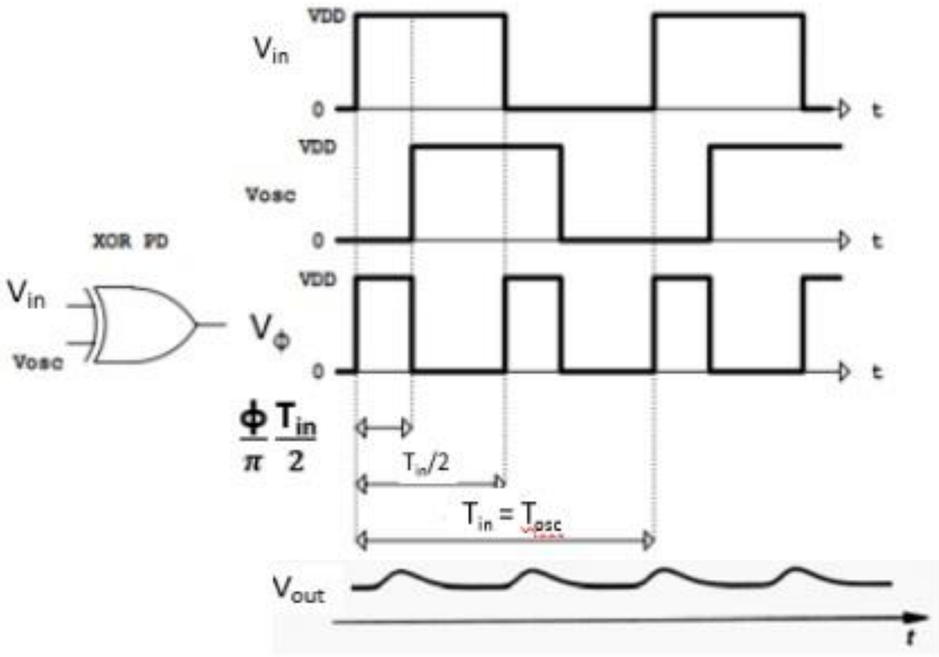
Digital Phase Detector

A simple digital phase detector is an XOR gate with logic low output (V_ϕ = 0V) and the logic high output ($V_\phi = V_{DD}$).
An example below shows the PLL is in the locked condition where V_{in} and V_{osc} are two phase-shifted periodic square-wave signals at the same frequency $\mathbf{f_{osc} = f_{in} = \frac{1}{T_{in}}}$, and with **50% duty ratios**. The **output of the phase detector is a periodic square-wave signal $V_\phi(t)$ at the frequency $2f_{in}$**, and with the duty ratio D_ϕ that depends on the phase difference $\boldsymbol{\phi(t) = [\phi_{osc}(t) - \phi_{in}(t)]}$ between V_{in} and V_{osc} ➔ $\mathbf{D_\phi = \frac{\phi}{\pi}}$ (for XOR)

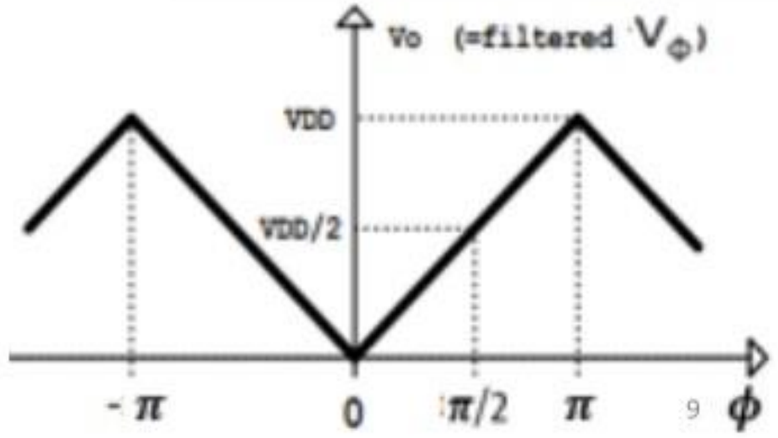


The dc component V_ϕ of the phase detector output can be found easily as the average of $V_\phi(t)$ over a period $\frac{T_{in}}{2}$

➔ $\mathbf{V_\phi = \frac{V_{DD}}{\pi}\phi = K_D\phi}$ $\mathbf{K_D}$ is called PD gain (for XOR)

where $\mathbf{K_D = \frac{V_{DD}}{\pi}}$ **volt/rad** for $0 \le \phi \le \pi$

The average output rise to $V_{out} = \frac{V_{DD}}{\pi}\Delta\Phi = 0 \rightarrow$ VDD when $\Delta\Phi$ goes from $0 \rightarrow \pi$. For $\Delta\Phi > \pi$, the average output begins to drop.

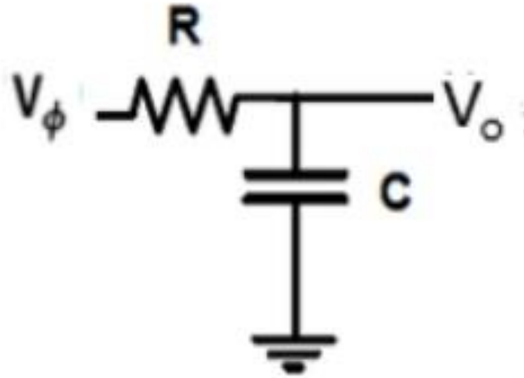


Loop Filter

The output $V_\phi(t)$ of the phase detector is filtered by the low-pass loop filter. **The purpose of the low-pass filter is to pass the dc and low-frequency portions of $V_\phi(t)$ and to attenuate high-frequency ac components at frequencies $2\pi f_{in}$.**
The simple RC filter has the transfer function:

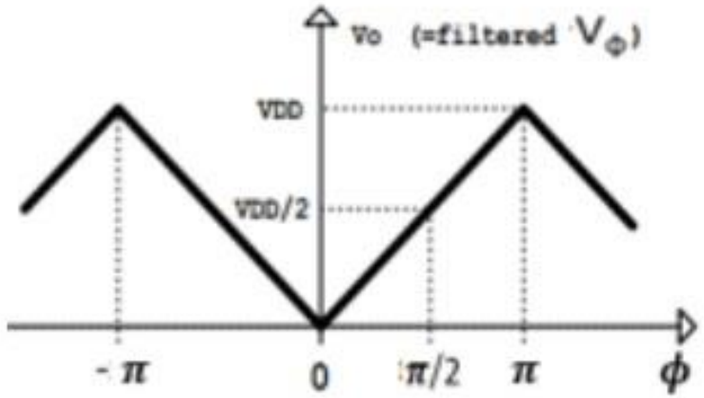
$$F(s) = \frac{1}{1+sRC} = \frac{1}{1+s/\omega_p}$$

where $\omega_p = \frac{1}{RC}$ and $f_p = \frac{\omega_p}{2\pi}$ is the cut-off frequency of the filter.



If $f_p << 2f_{in}$ ➔ the output of the filter V_{out} is approximately equal to the dc component V_ϕ of the phase detector output.
In practice, the high-frequency components are not completely eliminated and can be observed as high-frequency ac ripple around the dc or slowly-varying V_o.

In general, the filter output V_{out} as a function of the phase difference. Note that $V_{out} = 0$ if V_{in} and V_{osc} are in phase ($\phi = 0$), and that it reaches the maximum value $V_{out} = V_{DD}$ when the two signals are exactly out of phase ($\phi = \pi$).
For $0 \le \phi \le \pi$, V_o increases, and for $\phi > \pi$, V_o decreases. The characteristic of periodic in ϕ with period 2π.
The range $0 \le \phi \le \pi$ is the range where the PLL can operate in the locked condition.



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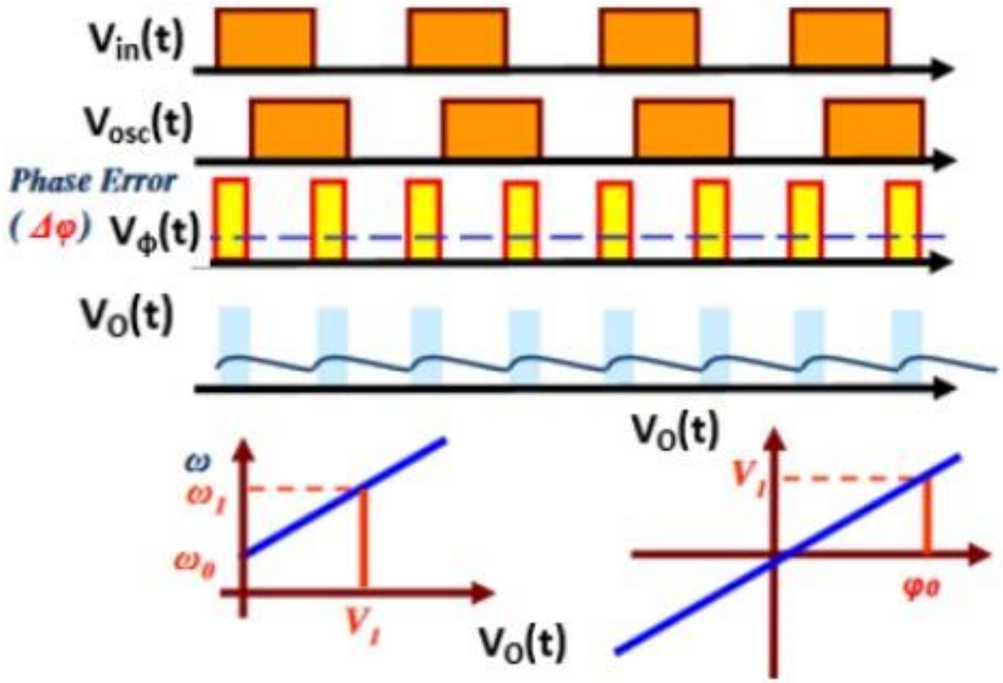
Voltage Controlled Oscillator (VCO)

In PLL applications, the VCO is treated as a linear, time-invariant system. To obtain an arbitrary output frequency (within the VCO tuning range), a finite V_{out} is required. Let's define $\phi_{osc} - \phi_{in} = \phi_o$.

The XOR function produces an output pulse whenever there is a phase misalignment. Suppose that an output frequency ω_1 is needed. From the upper right figure, we see that a control voltage V_1 will be necessary to produce this output frequency. The phase detector can produce this V_1 only by maintaining a phase offset ϕ at its input. In order to minimize the required phase offset or error, the PLL loop gain, $K_D K_O$, should be maximized, since $\phi = \frac{V_1}{K_D} = \frac{\omega_1 - \omega_0}{K_D K_O}$



Thus, a high **loop gain $K_D K_O$** is beneficial for reducing phase errors.

Note:

From Phase detector:

$V_1 = K_D \phi \rightarrow \phi = \frac{V_1}{K_D}$

From VCO:

$V_1 = \frac{\omega_1 - \omega_0}{K_O} \rightarrow \phi = \frac{V_1}{K_D} = \frac{\omega_1 - \omega_0}{K_D K_O}$

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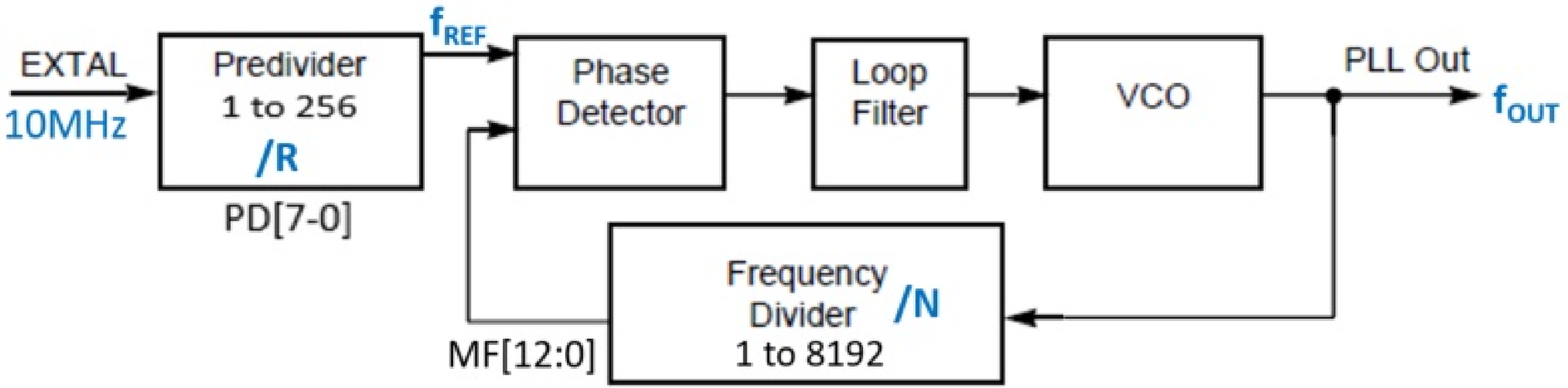
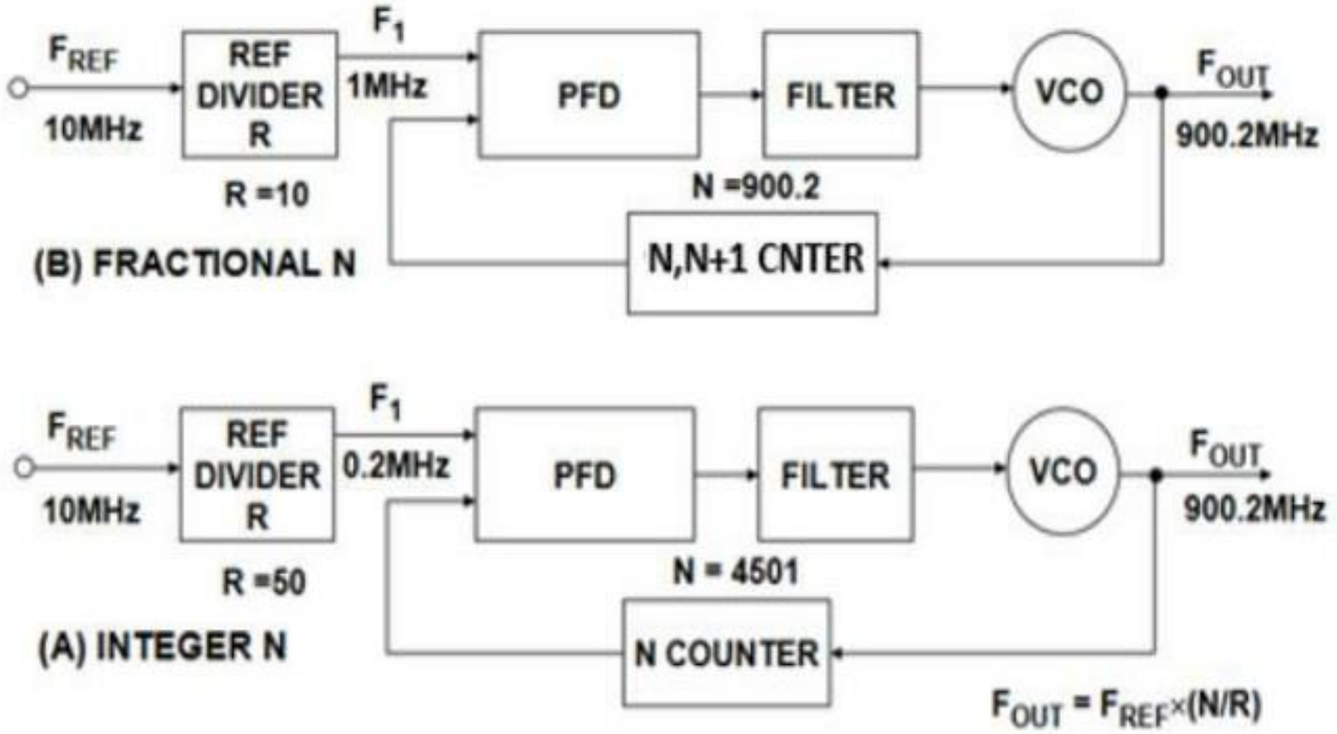
Integer-N Synthesizer

- The resolution of the output frequency is determined by the reference frequency applied to the phase detector. Step size or frequency resolution - the smallest frequency increment possible.
- To obtain a stable low frequency source is not easy, because a quartz crystal oscillating in kHz region is quite bulky and not practical. A sensible approach is to take a good stable crystal-based high frequency source and an integer-N synthesizer to divide it down.



Fractional-N Synthesizer

Fractional-N allows the resolution at the PLL output to be reduced to small fractions of the PFD frequency as shown below, where the PFD input frequency is 1 MHz. It is possible to generate output frequencies with resolutions of 100s of Hz, while maintaining a high PFD frequency. As a result the N-value is significantly less than for integer-N.



$$N_{EFF} = \frac{A(N)+B(N+1)}{A+B}$$

A: Cycle for N counter
B: Cycle for N+1 counter
A + B = 10
Toggling between the two integer division ratios, a fractional division ratio can be achieved by time-averaging the divider output.

$$N_{EFF} = \frac{8(900)+2(901)}{10} = 900.2$$

References

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Thank You