



SNS COLLEGE OF ENGINEERING
(Autonomous)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

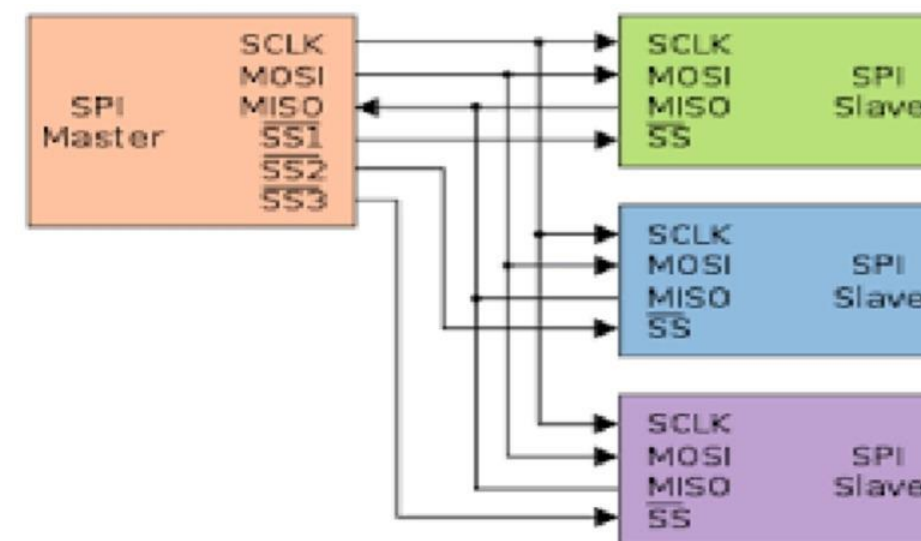


Unit 4-Embedded System
SPI,CAN

Serial Peripheral Interface (SPI) Bus:

The Serial Peripheral Interface Bus (SPI) is a synchronous bi-directional full duplex four wire serial interface bus. The concept of SPI is introduced by Motorola. SPI is a single master multi-slave system.

- It is possible to have a system where more than one SPI device can be master, provided the condition only one master device is active at any given point of time, is satisfied.
- SPI is used to send data between Microcontrollers and small peripherals such as shift registers, sensors, and SD cards.





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SPI REQUIRES FOUR SIGNAL LINES FOR COMMUNICATION. THEY ARE:

Master Out Slave In (MOSI):

Signal line carrying the data from master to slave device. It is also known as Slave Input/Slave Data In (SI/SDI) .

Master In Slave Out (MISO):

Signal line carrying the data from slave to master device. It is also known as Slave Output (SO/SDO).

Serial Clock (SCLK):

Signal line carrying the clock signals .

Slave Select (SS):

Signal line for slave device select. It is an active low signal.

The master device is responsible for generating the clock signal.

Master device selects the required slave device by asserting the corresponding slave devices slave select

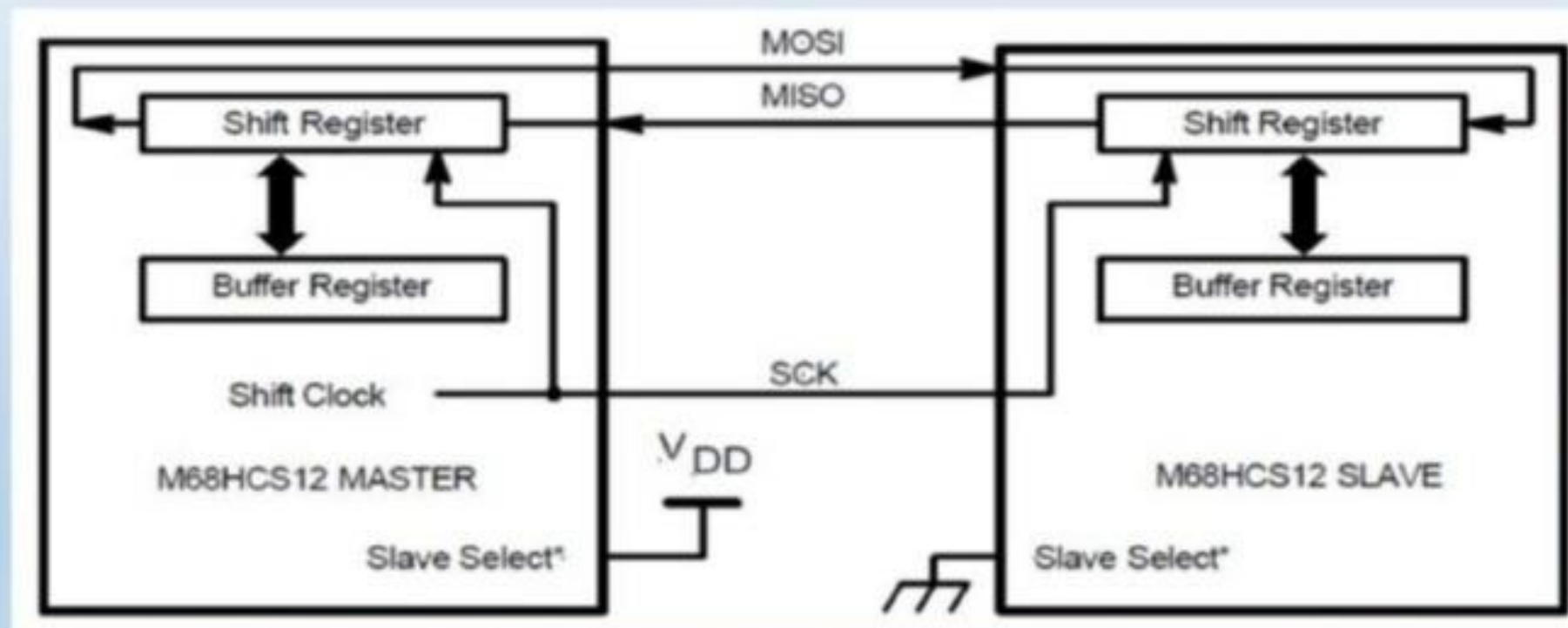


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- The data out line (MISO) of all the slave devices when not selected floats at high impedance state
- The serial data transmission through SPI Bus is fully configurable.
- SPI devices contain certain set of registers for holding these configurations.
- The Serial Peripheral Control Register holds the various configuration parameters like master/slave selection for the device, baudrate selection for communication, clock signal control etc.
- There status register holds the status of various conditions for transmission and reception.SPI
- works on the principle of „Shift Register“.
- The master and slave devices contain a special shift register for the data to transmit or receive.
- The size of the shift register is device dependent. Normally it is a multiple of 8.

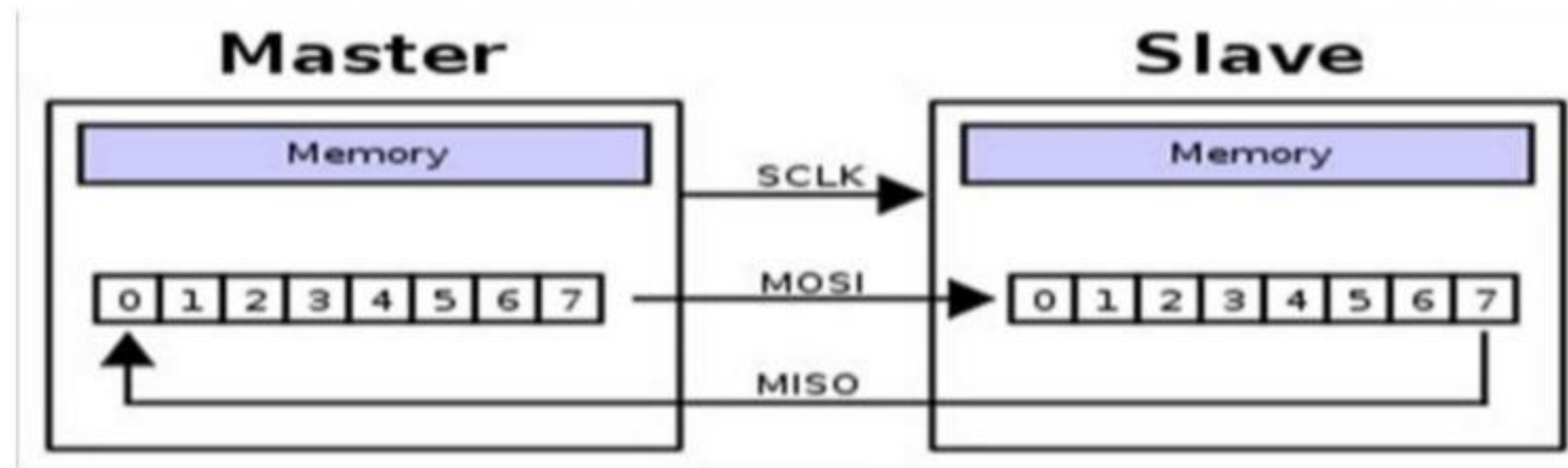
Operation of SPI protocol



Master/slave serial peripheral interface.

- During transmission from the master to slave, the data in the master's shift register is shifted out to the MOSI pin and it enters the shift register of the slave device through the MOSI pin of the slave device.

- At the same time the shifted out data bit from the slave device's shift register enters the shift register of the master device through MISO pin



Master shifts out data to Slave, and shift in data from Slave



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I2C Vs SPI

I2C	SPI
Speed limit varies from 100kbps, 400kbps, 1mbps, 3.4mbps depending on i2c version.	More than 1mbps, 10mbps till 100mbps can be achieved.
Half duplex synchronous protocol	Full Duplex synchronous protocol
Support Multi master configuration	Multi master configuration is not possible
Acknowledgement at each transfer	No Acknowledgement
Require Two Pins only SDA, SCL	Require separate MISO, MOSI, CLK & CS signal for each slave.
Addition of new device on the bus is easy	Addition of new device on the bus is not much easy a I2C
More Overhead (due to acknowledgement, start, stop)	Less Overhead
Noise sensitivity is high	Less noise sensitivity



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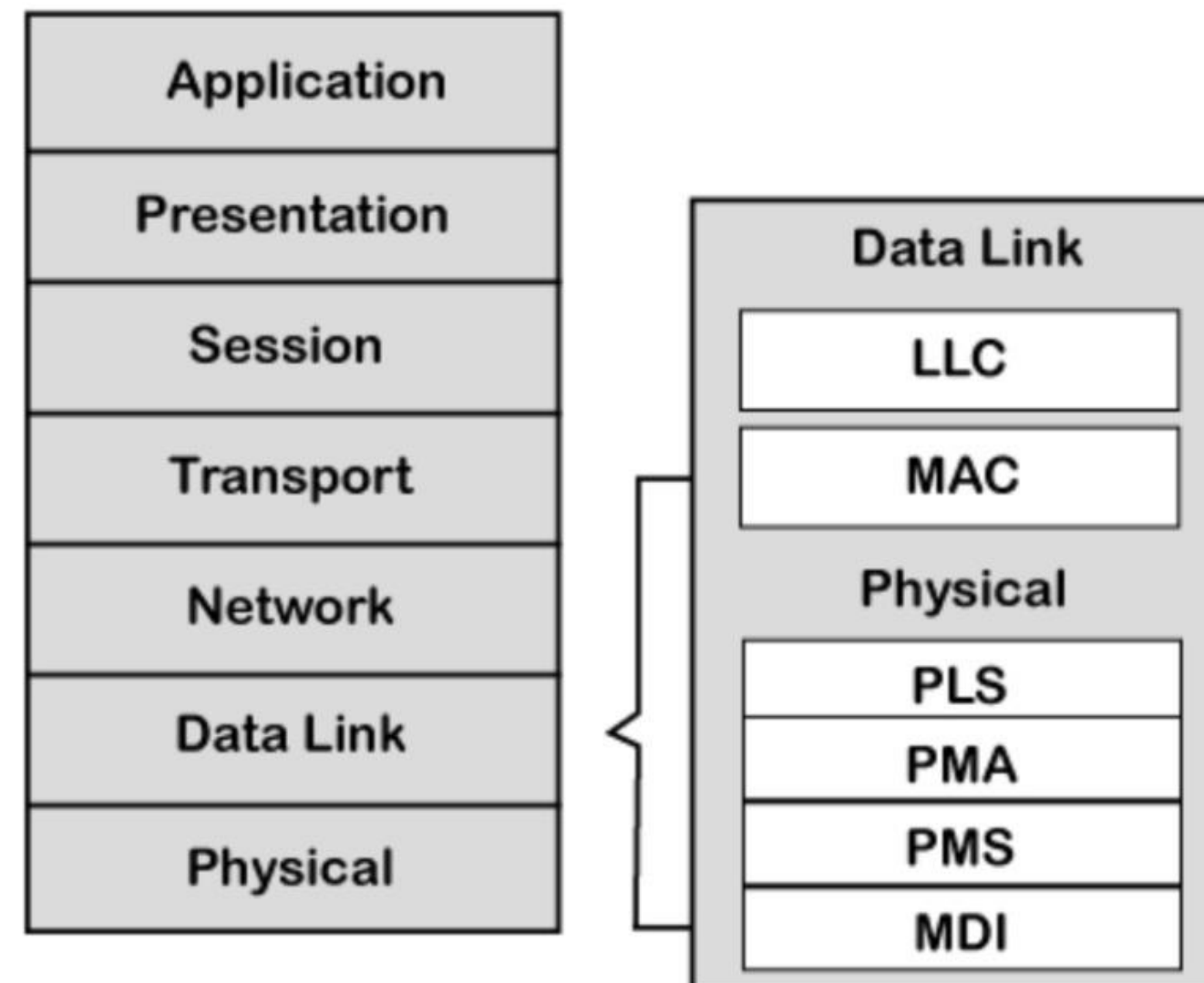
CAN BUS ;

- CAN stands for Controller Area Network protocol. It is a protocol that was developed by Robert Bosch in around 1986.
- The CAN protocol is a standard designed to allow the microcontroller and other devices to communicate with each other without any host computer.
- The feature that makes the CAN protocol unique among other communication protocols is the broadcast type of bus. Here, broadcast means that the information is transmitted to all the nodes.
- The CAN is a message-based protocol, which means that message carries the message identifier, and based on the identifier, priority is decided.
- It is a serial half-duplex and asynchronous type of communication protocol. The CAN is a two-wired communication protocol as the CAN network is connected through the two-wired bus.



CAN layered architecture

As we know that the OSI model partitions the communication system into 7 different layers. But the CAN layered architecture consists of two layers, i.e., data-link layer and physical layer.





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DATA LINK LAYER:

This layer is responsible for node to node data transfer. It allows you to establish and terminate the connection. It is also responsible for detecting and correcting the errors that may occur at the physical layer. Data-link layer is subdivided into two sub-layers:

MAC: MAC stands for Media Access Control. It defines how devices in a network gain access to the medium. It provides Encapsulation and Decapsulation of data, Error detection, and signaling.

LLC: LLC stands for Logical link control. It is responsible for frame acceptance filtering, overload notification, and recovery management.



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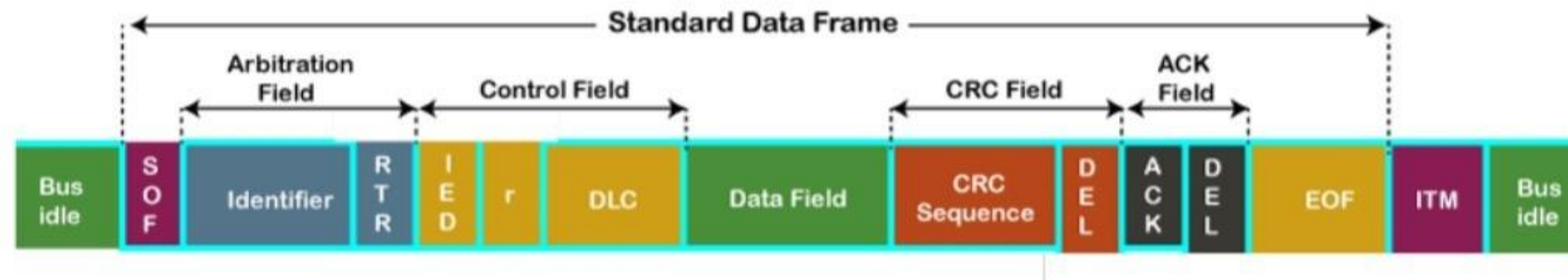
PHYSICAL LAYER:

- The physical layer is responsible for the transmission of raw data. It defines the specifications for the parameters such as voltage level, timing, data rates, and connector.
- CAN specifications define CAN protocol and CAN physical layer, which are defined in the CAN standard ISO 11898. ISO 11898 has three parts:
- **ISO 11898-1:** This part contains the specification of the Data-link layer and physical signal link.
- **ISO 11898-2:** This part comes under CAN physical layer for high speed CAN. The high-speed CAN allows data rate upto 1 Mbps used in the power train and the charges area of the vehicle.

- **ISO 11898-3:** This part also comes under CAN physical layer for low-speed CAN. It allows data rate upto 125 kbps, and the low speed CAN is used where the speed of communication is not a critical factor.
- **CiA DS-102:** The full form of CiA is CAN in Automation, which defines the specifications for the CAN connector.

CAN FRAMING:

Let's understand the structure of the CAN frame





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SOF: SOF stands for the start of frame, which indicates that the new frame is entered in a network. It is of 1 bit.

Identifier: A standard data format defined under the CAN 2.0 A specification uses an 11-bit message identifier for arbitration. Basically, this message identifier sets the priority of the data frame.

RTR: RTR stands for Remote Transmission Request, which defines the frame type, whether it is a data frame or a remote frame. It is of 1-bit

Control field: It has user-defined functions.

- 1.IDE:** An IDE bit in a control field stands for identifier extension. A dominant IDE bit defines the 11-bit standard identifier, whereas recessive IDE bit defines the 29-bit extended identifier.
- 2.DLC:** DLC stands for Data Length Code, which defines the data length in a data field. It is of 4 bits.
- 3.Data field:** The data field can contain upto 8 bytes.



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CRC field: The data frame also contains a cyclic redundancy check field of 15 bit, which is used to detect the corruption if it occurs during the transmission time. The sender will compute the CRC before sending the data frame, and the receiver also computes the CRC and then compares the computed CRC with the CRC received from the sender. If the CRC does not match, then the receiver will generate the error.

ACK field: This is the receiver's acknowledgment. In other protocols, a separate packet for an acknowledgment is sent after receiving all the packets, but in case of CAN protocol, no separate packet is sent for an acknowledgment.

EOF: EOF stands for end of frame. It contains 7 consecutive recessive bits known End of frame.



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Applications of CAN protocol;

- Automotive (passenger vehicles, trucks, buses)
- Electronic equipment for aviation and navigation
- Industrial automation and mechanical control
- Elevator and escalators
- Building automation
- Medical instruments and equipment
- Marine, medical, industrial, medical



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THANK YOU