Unit 2- ARM Processors and Peripherals

Block Diagram of ARM Cortex M3 MCU

ARM Cortex M3 MCU

- The ARM Cortex™-M3 processor, the first of the Cortex generation of processors released by ARM in 2006, was primarily designed to target the 32-bit microcontroller market.
- The Cortex-M3 processor provides excellent performance at low gate count and comes with many new features previously available only in high-end processors.
- The Cortex-M3 addresses the requirements for the 32-bit embedded processor

The Cortex-M3 addresses the requirements for the 32-bit embedded processor market in the following ways: ¬ Greater performance efficiency: allowing more work to be done without increasing the frequency or power requirements

- Low power consumption: enabling longer battery life, especially critical in portable products including wireless networking applications
- Enhanced determinism: guaranteeing that critical tasks and interrupts are serviced as quickly as possible and in a known number of cycles
- Improved code density: ensuring that code fits in even the smallest memory footprints
- Ease of use: providing easier programmability and debugging for the growing number of 8-bit and 16-bit users migrating to 32 bits

- Lower cost solutions: reducing 32-bit-based system costs close to those of legacy 8-bit and 16-bit devices and enabling low-end, 32-bit microcontrollers to be priced at less than US$1 for the first time
- Wide choice of development tools: from low-cost or free compilers to full featured development suites from many development tool vendors

ABOUT ARM CORTEX:

- Cortex-M3 processor-based microcontrollers can be easily programmed using the C language and are based on a well-established architecture, application code can be ported and reused easily, reducing development time and testing costs.
- Additionally, the Cortex-M3 processor introduces a number of features and technologies that meet the specific requirements of the microcontroller applications, such as non maskable interrupts for critical tasks, highly deterministic nested vector interrupts, atomic bit manipulation, and an optional Memory Protection Unit (MPU).
- These factors make the Cortex-M3 processor attractive to existing ARM processor users as well as many new users considering use of 32-bit MCUs in their products.

INSTRUCTION SETS IN ARM CORTEX:

Two different instruction sets are supported on the ARM processor:

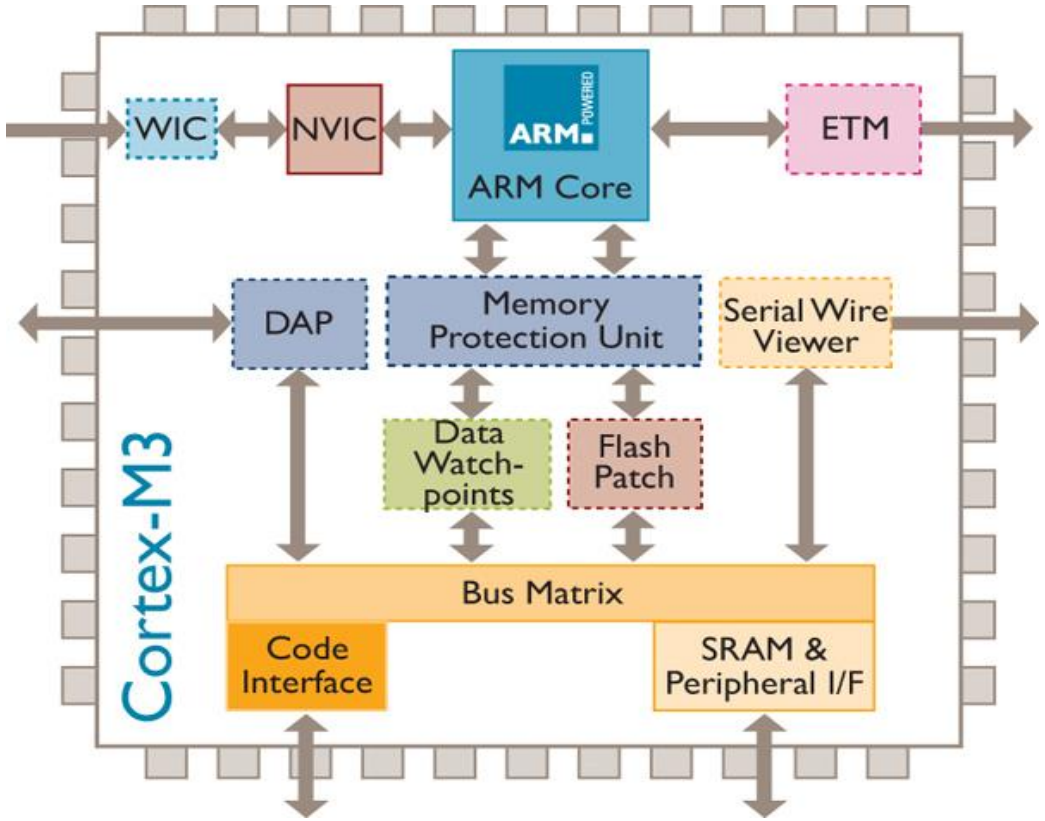
- The ARM instructions that are 32 bits and Thumb instructions that are 16 bits.
- During program execution, the processor can be dynamically switched between the ARM state and the Thumb state to use either one of the instruction sets.
- The Thumb instruction set provides only a subset of the ARM instructions, but it can provide higher code density. It is useful for products with tight memory requirements.

Features of ARM Cortex M3:

The ARM Cortex-M3 features:

- **32-bit RISC architecture** with Thumb-2 for high performance and code efficiency.
- **NVIC** for low-latency interrupt handling.
- **Memory Protection Unit (MPU)** for safety.
- **Bit-banding** for atomic memory access.
- Low power modes for energy efficiency.
- Integrated debug (JTAG/SWD) and timers for ease of development.

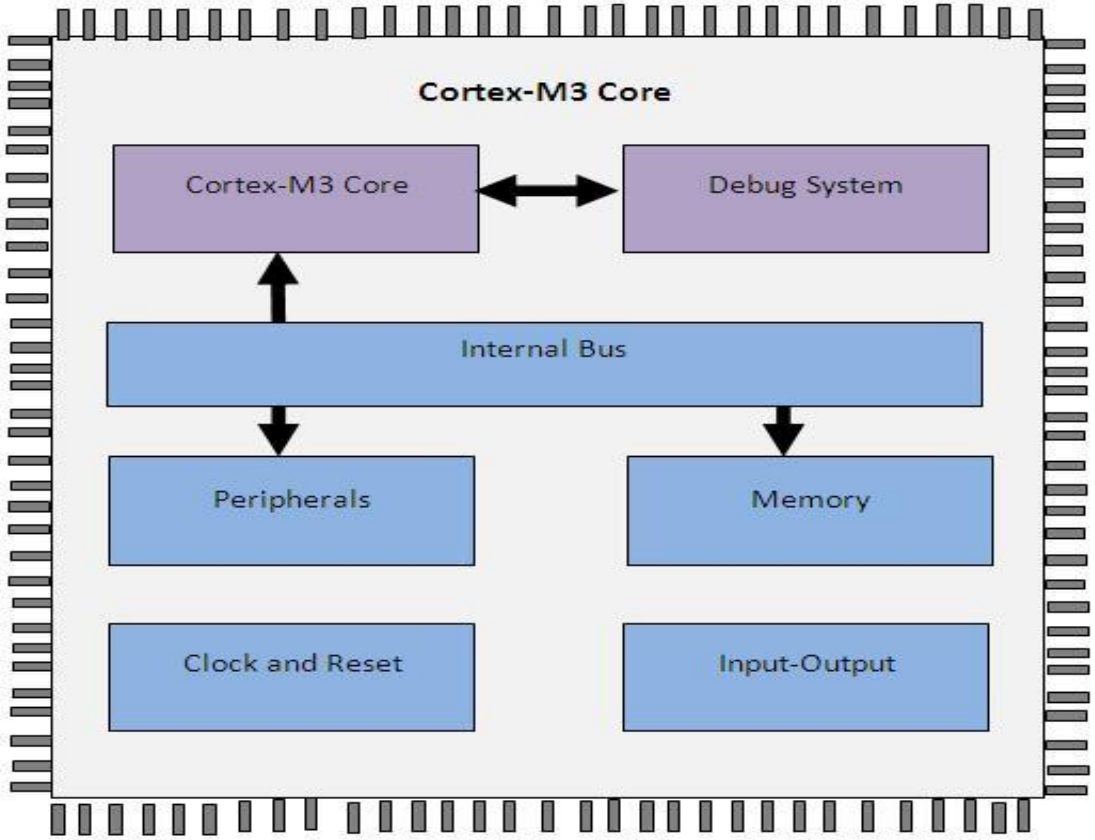
BLOCK DIAGRAM:



ARM CORTEX M3 ARCHITECTURE

The ARM Cortex-M3 processor has been designed 'from the ground up' to prov ide optimal performance and power consumption within a minimal memory system. To achieve this the core executes only the Thumb-2 instruction set. The design is based on a 3-stage pipeline Harvard architecture that maximizes memory utilization through the support of unaligned date storage, and single cycle atomic bit manipulation. The highly revised architecture implements hardware div ide and single-cycle multiply. The ARM Cortex-M3 uses 33k gates for the processing core and 60k gates total, including many closed system peripherals. The ARM Cortex-M3 processor reduces the number of pins required for debug from five to one, by implementing a Single Wire Debug. For system trace, the processor integrates an optional ETM alongside data watch points that can be configured to trigger on specific system events. To enable simple and cost-effective profiling of these system events a SWV (Seria l Wire Viewer) can export streams of standard ACSII data through a single pin. Flash Patch technology offers device and system developers the ability to patch errors in code from ROM to SRAM or Flash during both debug and run-time

ARM CORTEX M3 MICROCONTROLLER ARCHITECTURE:



ARM CORTEX M3 APPLICATION:

- **Consumer Electronics:** Smart appliances, wearables, and gaming devices.
- **Industrial Automation:** Motor control, robotics, and process controllers.
- **Medical Devices:** Portable monitors, infusion pumps, and diagnostic equipment.
- **Automotive Systems:** Engine control, airbag systems, and in-vehicle infotainment.
- **IoT Devices:** Smart home systems, sensors, and wireless communication modules

Thank you