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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## **CPU PERFORMANCE IN EMBEDDED SYSTEMS**

- Multi Core Processors
- Pipelining
- Cache



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#### MULTI CORE PROCESSORS

##### Definition:

CPUs with multiple cores (processing units) integrated into a single chip.

##### Purpose:

- **Parallel Processing:** Each core can execute a separate task simultaneously, increasing overall processing capacity.
- **Improved Multitasking:** Multiple tasks or threads can run concurrently without affecting each other.
- **Energy Efficiency:** Distributing the workload across multiple cores often reduces the need for high clock speeds, saving power.



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#### PIPELINE PROCESSING

##### Definition:

- A method where instruction execution is divided into stages (e.g., fetch, decode, execute), allowing multiple instructions to be processed simultaneously in different stages.

##### Purpose:

- **Improved Throughput:** Instead of waiting for one instruction to finish, the CPU processes parts of multiple instructions at the same time.
- **Efficient Resource Usage:** Each stage of the pipeline operates continuously, minimizing idle CPU cycles.



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**Working**

- Instruction 1: **Fetch Stage**  
(fetches the instruction from memory).
- Instruction 2: **Decode Stage**  
(interprets the instruction).
- Instruction 3: **Execute Stage**  
(performs the operation).



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## **CACHE MEMORY**

### **Definition:**

- A small, high-speed memory located close to the CPU that stores frequently accessed data and instructions.

### **Purpose:**

- **Faster Access:** Reduces the time the CPU spends waiting for data from slower main memory.
- **Improved System Performance:** High cache hit rates significantly boost CPU efficiency.



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**Thank you**