SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: Microcontroller Programming And Interfacing
Subcode:23ECB202
Unit-II

CLASSIFICATION OF INSTRUCTIONS AND IO PORT PROGRAMMING/ Peripherals of PIC- ADC, DAC

ANALOG to DIGITAL CONVERTOR (ADC)

ADC Channel	Pin
Channel 0	RA0/AN0 (Port A)
Channel 1	RA1/AN1 (Port A)
Channel 2	RA2/AN2/VRef- (Port A)
Channel 3	RA3/AN3/VRef+ (Port A)
Channel 4	RA5/AN4 (Port A)
Channel 5	RE0/AN5 (Port E)
Channel 6	RE1/AN6 (Port E)
Channel 7	RE2/AN7 (Port E)

Registers used in ADC

- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)

A/D Control Register 0 (ADCON0)

The ADCON0 register, shown in the below image, controls the operation of the A/D module i.e. Used to Turn ON the ADC, Select the Sampling Freq, and Start the conversion.

ADCON0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

- **ADCS1-ADCS0:** A/D Conversion Clock Select bits. These bits are based on ADCON1 Reister's ADCS2 bit.

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

ADC

CHS2-CHS0: Analog Channel Select bits

000	=	Channel	0	(AN0)
001	=	Channel	1	(AN1)
010	=	Channel	2	(AN2)
011	=	Channel	3	(AN3)
100	=	Channel	4	(AN4)
101	=	Channel	5	(AN5)
110	=	Channel	6	(AN6)

111 = Channel 7 (AN7)

ADC

GO/DONE: A/D Conversion Status bit

When ADON = 1:

- 1 = A/D conversion in progress (setting this bit starts the A/D conversion, which is automatically cleared by hardware when the A/D conversion is complete)
- 0 = A/D conversion not in progress

ADON: A/D On bit

- 1 = A/D converter module is powered up
- 0 = A/D converter module is shut off and consumes no operating current

A/D Control Register 1 (ADCON1)

The ADCON1 register, shown below, configures the functions of the port pins, i.e. used to configure the GPIO pins for ADC. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

ADCON1 REGISTER

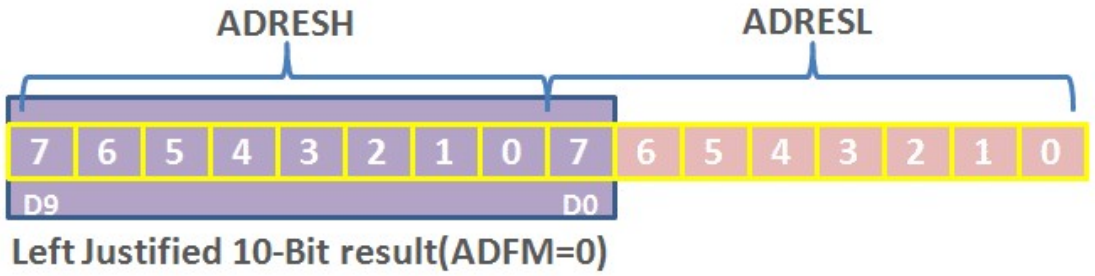
R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

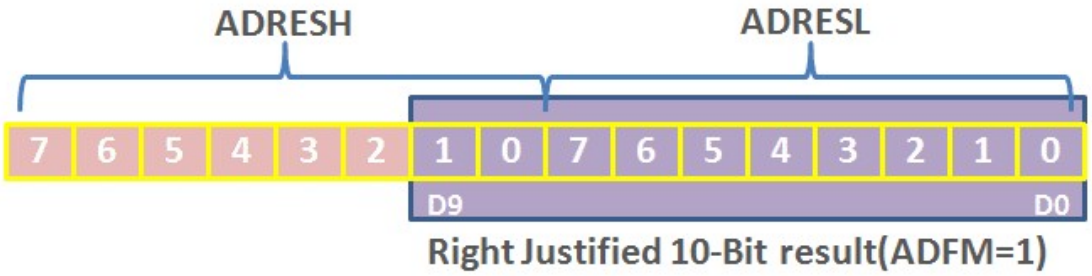
A/D Control Register 1 (ADCON1)

ADFM: A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.





ADCS2 A/D Conversion Clock Select Bit

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

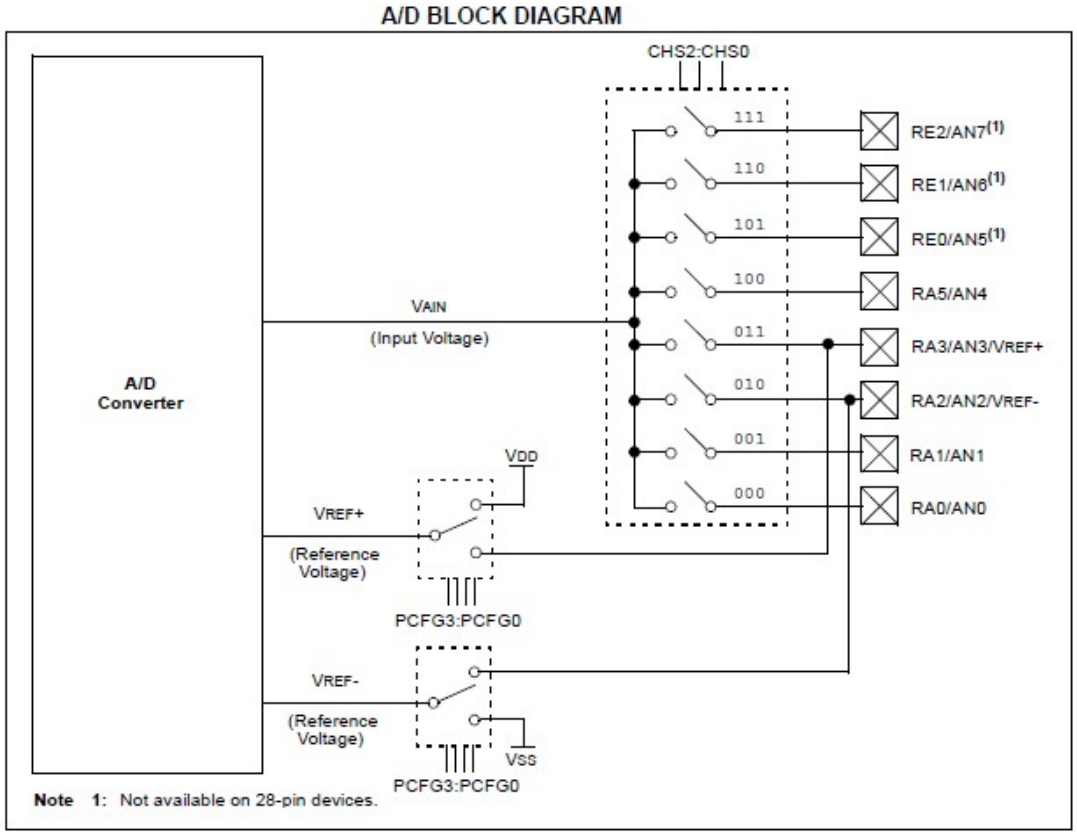
- **PCFG3-PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O
C/R = # of analog input channels/# of A/D voltage references

A/D Block Diagram

- The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/DONE bit (ADCON0) is cleared and the A/D interrupt flag bit ADIF is set.
- The block diagram of the A/D module is shown in Fig. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.



A/D Conversion

1. Configure the A/D module:

- Configure analog pins/voltage reference and
- digital I/O (ADCON1)
- Select A/D input channel (ADCON0)
- Select A/D conversion clock (ADCON0)
- Turn on A/D module (ADCON0)

2. Configure A/D interrupt (if desired):

- Clear ADIF bit
- Set ADIE bit
- Set PEIE bit
- Set GIE bit

A/D Conversion

3. Wait the required acquisition time.
4. Start conversion:
   Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete by either:
   Polling for the GO/DONE bit to be cleared (interrupts disabled);
OR
   Waiting for the A/D interrupt
6. Read A/D Result register pair
   (ADRESH:ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2
   as required. The A/D conversion time per bit is defined as TAD.