DIGITAL ELECTRONICS:

REALIZATION OF GATES USING NAND GATE

SNS COLLEGE OF ENGINEERING

Kurumbapalayam (PO), Coimbatore – 641 107

An Autonomous Institution

Accredited by NAAC – UGC with 'A' Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

REALIZATION OF GATES USING NAND GATE

Dr.G.Arthy
Assistant Professor
Department of EEE
SNS College of Engineering

INTRODUCTION TO UNIVERSAL GATES

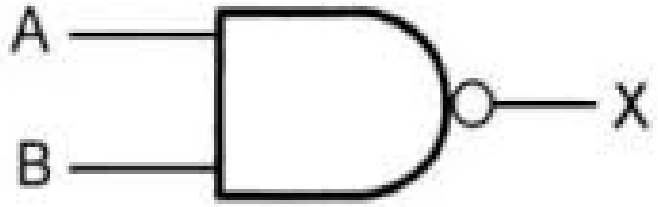
- What are Universal Gates?
- Why?

What are Universal Gates?

- NAND gate
- NOR gate

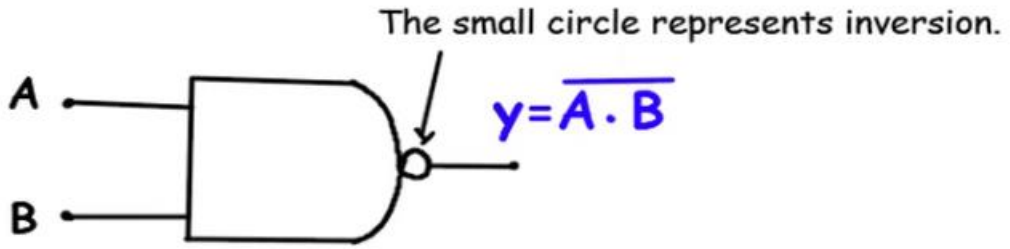
NAND Gate

$$X = \overline{A.B}$$

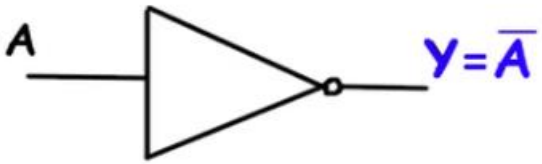


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

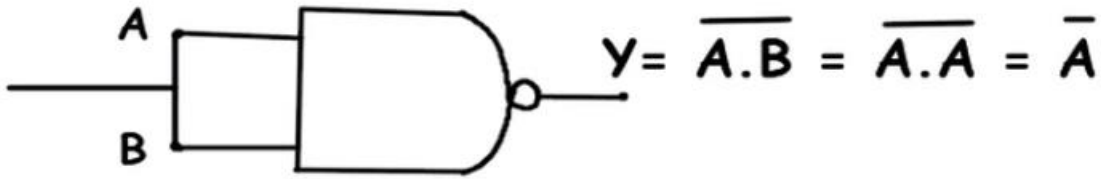
NAND as NOT



NAND gate
Symbol

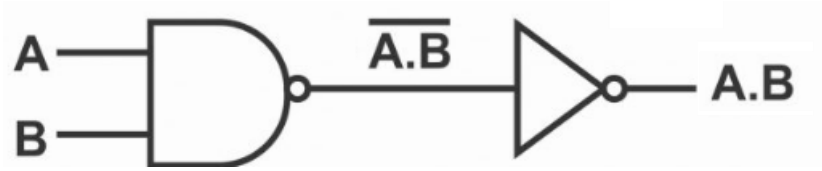


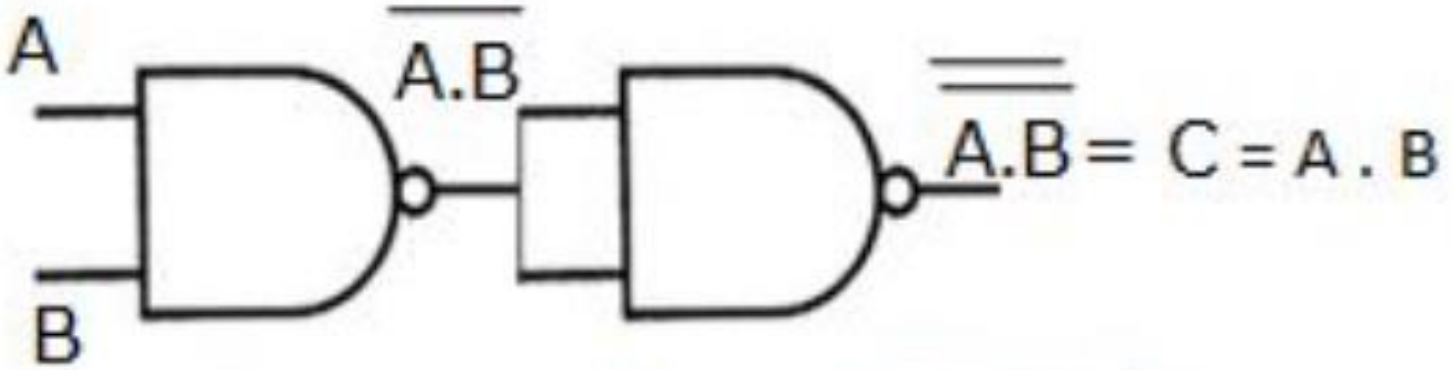
NOT gate
Symbol



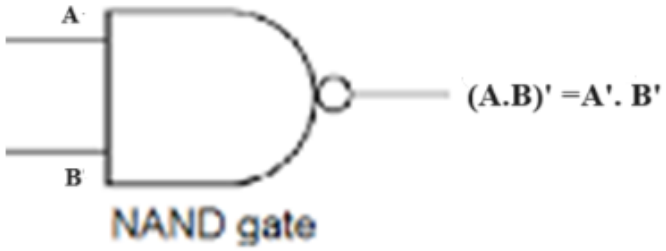
NOT Gate using NAND Gate

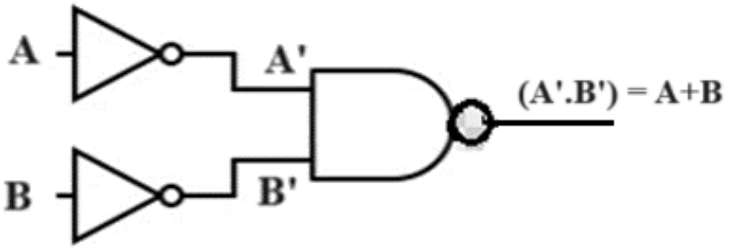
NAND as AND

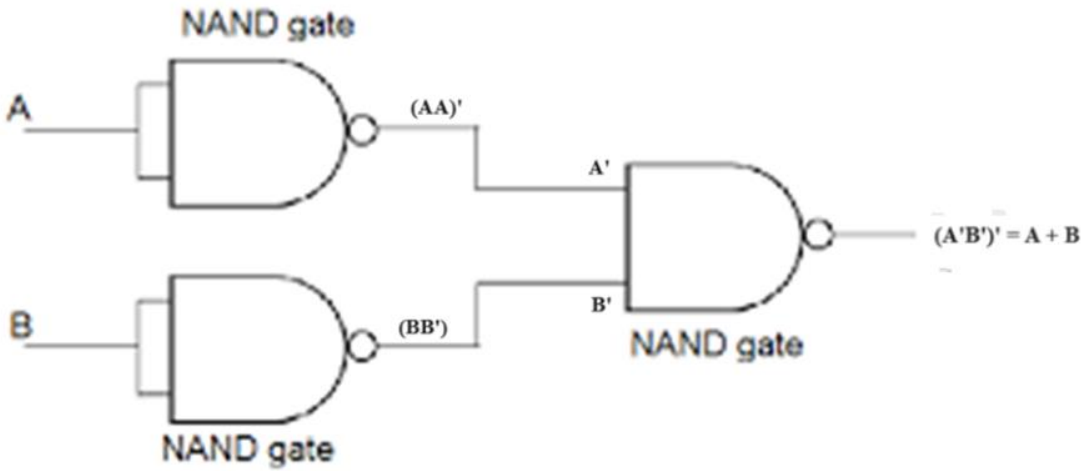




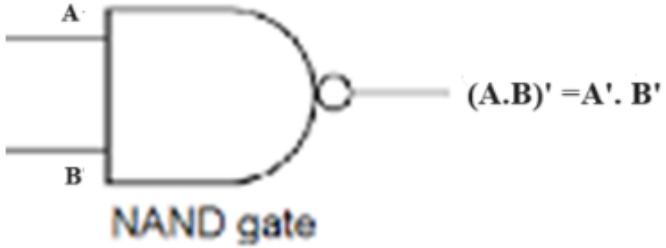
NAND as OR

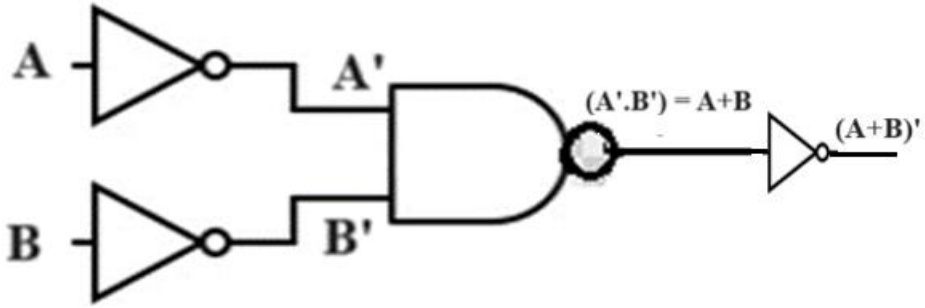

A
B
(A.B)' =A'. B'
NAND gate

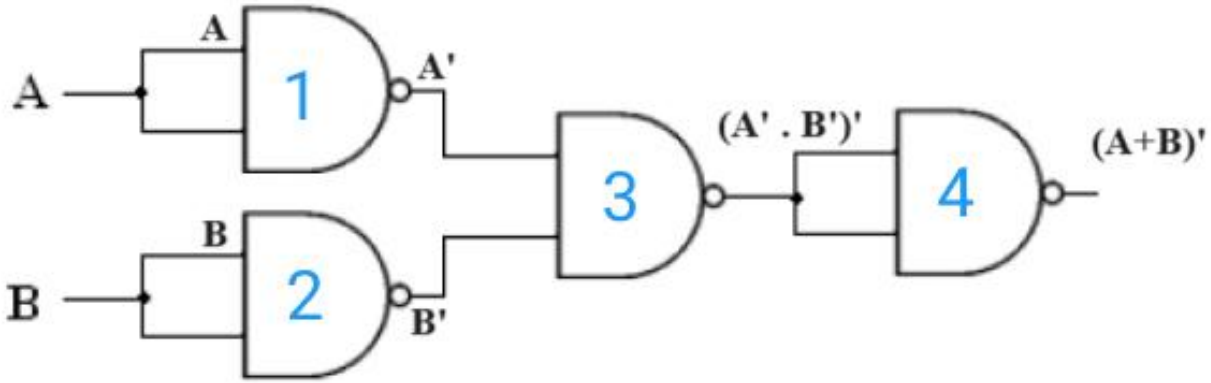

A
A'
(A'.B') = A+B
B
B'


NAND gate
A
(AA)'
A'
(A'B')' = A + B
B
(BB')
B'
NAND gate
NAND gate

NAND as NOR







Assessment 1

1. How many NAND gates are required to implement one NOR gate.

2. Draw the EXOR gate using NAND gates.


Thank
you