## REALIZATION OF GATES USING NOR GATE



# **SNS COLLEGE OF ENGINEERING**



Kurumbapalayam (PO), Coimbatore – 641 107 An Autonomous Institution

Accredited by NAAC – UGC with 'A' Grade Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

#### **DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

### **REALIZATION OF GATES USING NOR GATE**

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Realization of gates using NOR gate /Dr.G.Arthy/AP/EEE



## **INTRODUCTION TO UNIVERSAL GATES**



• What are Universal Gates?

• Why?



# What are Universal Gates?



• NAND gate

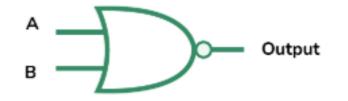
• NOR gate







#### 2- Input NOR Gate



#### Truth Table

Input A	Input B	0 = (A + B)'
0	0	1
0	1	0
1	0	0
1	1	0

#### 3 Input NOR Gate



#### **Truth Table**

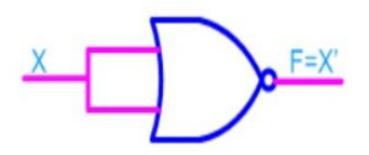
Input A	Input B	Input C	X = (A,B,C)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



# **NOR as NOT**



Input	Output	Rule
(X+X)'	= X'	Idempotent



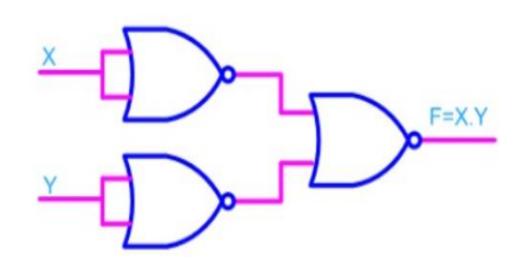


# NOR as AND



#### Implementing AND using NOR gates

Input	Output	Rule
((X+X)'+(Y+Y) ')'	=(X'+Y')	Idempotent
	= X".Y"	DeMorgan
	= (X.Y)	Involution

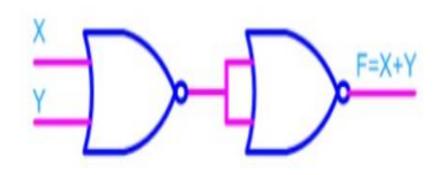




# NOR as OR



Input	Output	Rule
((X+Y)'+(X+Y)')'	= ((X+Y)')'	Idempotent
	= X+Y	Involution

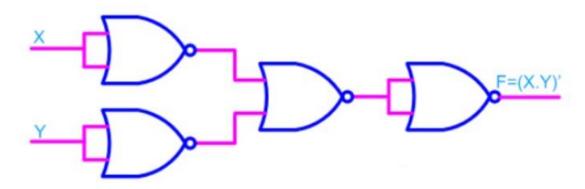




### NAND USING NOR



Input	Output	Rule
((X+Y)'+(X+Y)')'	=((X+Y)')'	Idempotent
	= X + Y	Involution
	= (X+Y)'	Idempotent





## **EXOR USING NOR**



The output of the XOR gate is given by,

 $Y = \overline{A}B + A\overline{B} = A \oplus B$ 

Taking the double complement on the right-hand side, we get,

$$Y = \overline{\overline{A \oplus B}} = \overline{A \odot B}$$

$$\Rightarrow Y = \overline{AB + \overline{A} \cdot \overline{B}}$$

$$\Rightarrow Y = \overline{AB + (\overline{A + B})}$$

$$\Rightarrow Y = \overline{\overline{AB} + (\overline{A + B})}$$

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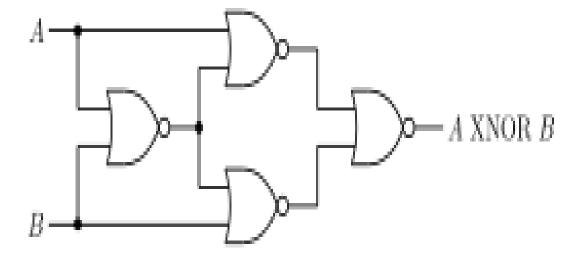
Hence, this Boolean expression is equivalent to the output of the XOR gate





## **EXNOR USING NOR**

$$\begin{split} Y &= \overline{\overline{A + (\overline{A + B})}} + \overline{B + (\overline{A + B})} \\ Y &= \overline{\overline{A + (\overline{A + B})}} &= \overline{\overline{B + (\overline{A + B})}} \\ Y &= \overline{A + (\overline{A + B})} &= \overline{B + (\overline{A + B})} \\ Y &= (A + (\overline{A + B})) \cdot (B + (\overline{A + B})) \\ Y &= (A + (\overline{A} \cdot \overline{B})) (B + (\overline{A} \cdot \overline{B})) \\ Y &= (A + \overline{A}) (A + \overline{B}) (\overline{A} + B) (B + \overline{B}) \\ Y &= (A + \overline{A}) (A + \overline{B}) (\overline{A} + B) \\ Y &= (A + \overline{A} + \overline{A} \cdot \overline{B} + A \cdot B + B \cdot \overline{B}) \\ \vdots Y &= A \cdot \overline{A} + \overline{A} \cdot \overline{B} + A \cdot B + B \cdot \overline{B} \\ & \therefore Y &= A \cdot B + \overline{A} \cdot \overline{B} \end{split}$$









1. How many NOR gates are required to implement one EXOR gate.

2. Draw the NAND gate using NOR gates.





