DIGITAL ELECTRONICS:
SR LATCH

SNS COLLEGE OF ENGINEERING

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An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SR LATCH

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SR LATCH

- ✓ Latches are digital circuits that store a single bit of information and hold its value until it is updated by new input signals.
- ✓ They are used in digital systems as temporary storage elements to store binary information.
- ✓ Latches are level-sensitive devices. Latches are useful for the design of the asynchronous sequential circuit. Latches are sequential circuit with two stable states.

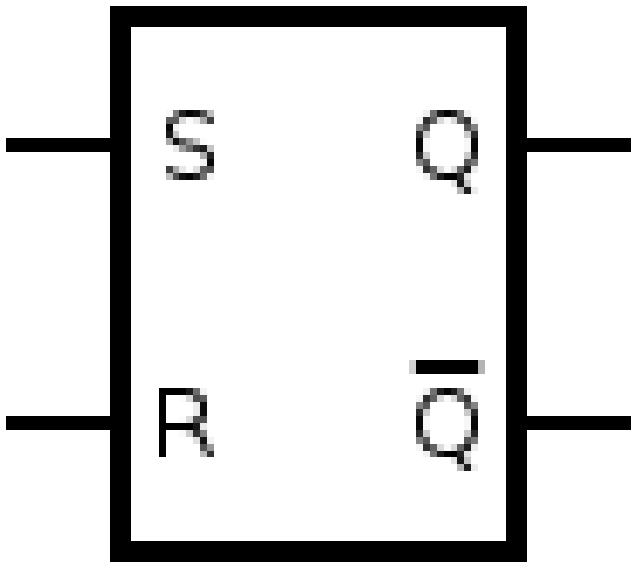
SR LATCH

APPLICATIONS

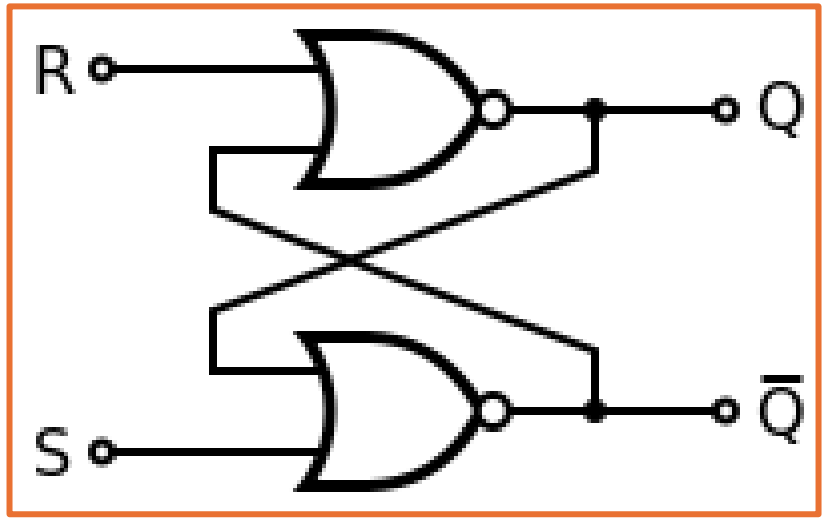
- ✓ Latches are widely used in digital systems for various applications, including data storage, control circuits, and flip-flop circuits. They are often used in combination with other digital circuits to implement sequential circuits, such as state machines and memory elements.

SR LATCH

- ✓ SR (Set-Reset) Latch – They are also known as preset and clear states. The SR latch forms the basic building blocks of all other types of flip-flops.



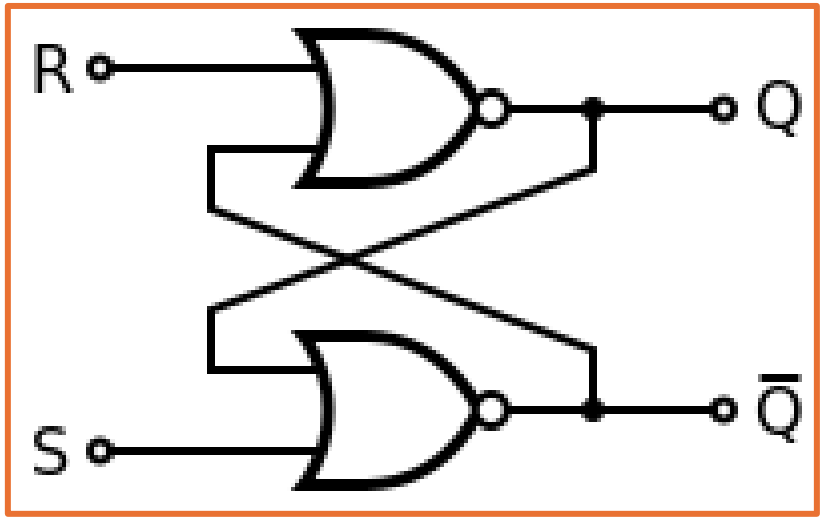
SR LATCH WITH NOR GATE



SR Latch is a circuit with:

- ✓ (i) 2 cross-coupled NOR gate or 2 cross-coupled NAND gate.
- ✓ (ii) 2 input S for SET and R for RESET.
- ✓ (iii) 2 output Q, Q'.

SR LATCH WITH NOR GATE



When S=0, R=1→ Q = 0 and Q' = 1

When S=0, R=0→ Q = 0 and Q' = 1 (Memory)

When S=1, R=0→ Q = 1 and Q' = 0

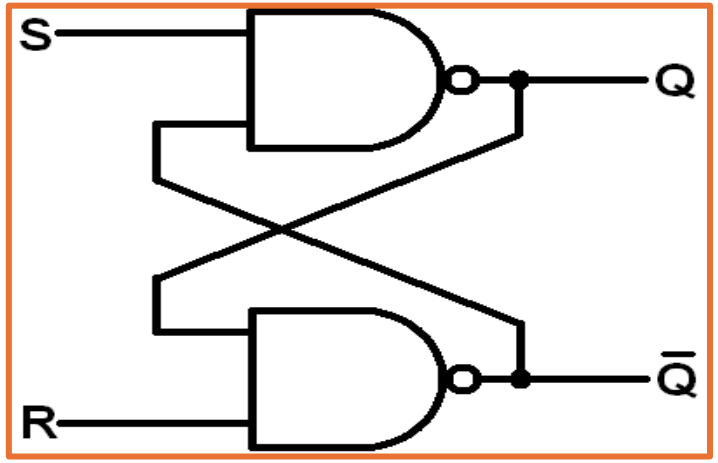
When S=0, R=0→ Q = 1 and Q' = 0(Memory)

When S=1, R=1→ Q = 0 and Q' = 0(Invalid)

SR Latch Truth Table

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	unstable	

SR LATCH WITH NAND GATE



When S=0, R=1→ Q = 1 and Q' = 0

When S=1, R=1→ Q = 1 and Q' = 0 (Memory)

When S=1, R=0→ Q = 0 and Q' = 1

When S=1, R=1→ Q = 0 and Q' = 1(Memory)

When S=0, R=0→ Q = 1 and Q' = 1(Invalid)

SR Latch Truth Table

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	0	unstable	
0	1	1	0
1	0	0	1
1	1	unchanged	

Assessment

1. What is the purpose of a Set-Reset (SR) latch in digital electronics?

2. In an SR latch, what is the state when both the Set (S) and Reset (R) inputs are asserted simultaneously?


Thank
you