DIGITAL ELECTRONICS:
JK FLIPFLOP

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An Autonomous Institution

Accredited by NAAC – UGC with 'A' Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

JK FlipFlop

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JK FLIPFLOP

- ✓ The “JK flip flop,” also known as the Jack Kilby flip flop, is a sequential logic circuit designed by Jack Kilby during his tenure at Texas Instruments in the 1950s. This flip flop serves the purpose of storing and manipulating binary information within digital systems.
- ✓ JK flip flop is an improved clocked SR flip flop.

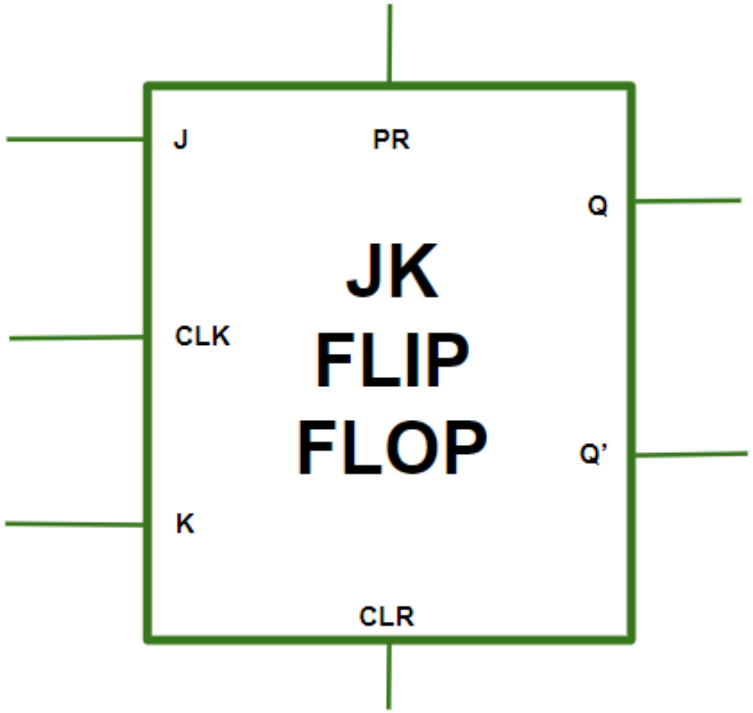
JK FLIPFLOP

APPLICATIONS

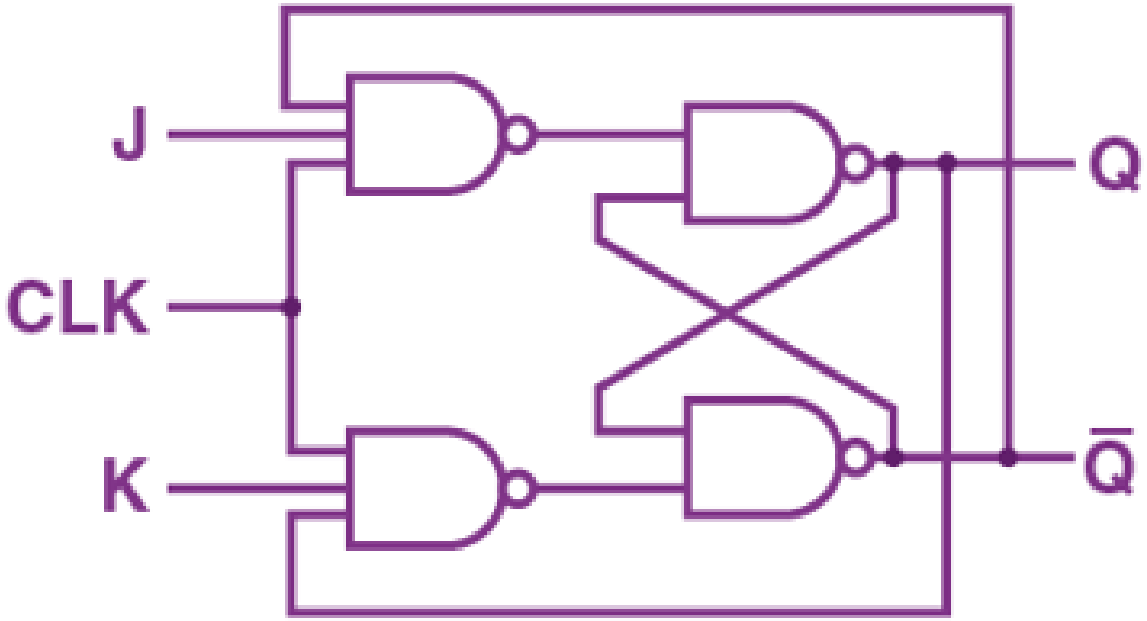
- ✓ Counters
- ✓ Shift Registers
- ✓ Memory Units
- ✓ Frequency Division

JK FLIP FLOP

- ✓JK flip flop operates on sequential logic principle, where the output is dependent not only on the current inputs but also on the previous state.
- ✓There are two inputs in JK Flip Flop Set and Reset denoted by J and K. It also has Output and complement of Output denoted by Q and Q̄.
- ✓The internal circuitry of a JK Flip Flop consists of a combination of logic gates, usually NAND gates.



JK FLIPFLOP WITH NAND GATE



JK FLIPFLOP TRUTH TABLE

CLK	J	K	Q n	Q n+1	Q n+1
0	X	X	0/1	0/1	Q n
↑	0 0	0 0	0 1	0 1	Q n
↑	0 0	1 1	0 1	0 0	0
↑	1 1	0 0	0 1	1 1	1
↑	1 1	1 1	0 1	1 0	Q n’

JK FLIPFLOP CHARACTERISTIC TABLE

The characteristic table for this type of flip-flop exhibits the transition of present state to next state based on the input conditions and clock triggers.

Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

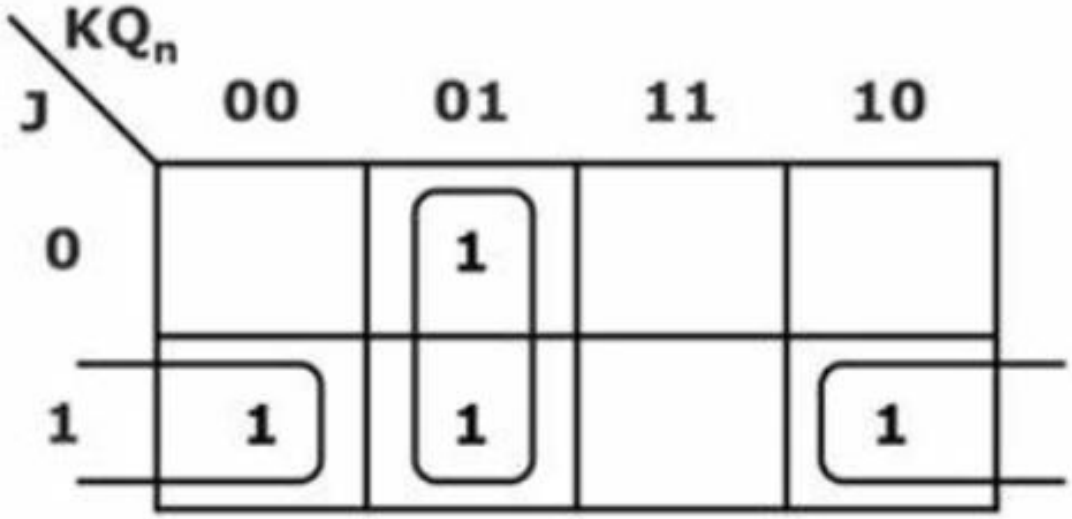
JK FLIPFLOP EXCITATION TABLE

The excitation table of SR flip-flop indicate the excitations required to take the flip-flop from the present state to the next state.

Q Output		Inputs	
Present State	Next State	J_n	K_n
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

JK FLIPFLOP CHARACTERISTIC EQUATION

The characteristic equation is an algebraic expression for the characteristic table's binary information. It specifies the value of the next state of a flip-flop in terms of its present state and present excitation.



$\therefore$ Characterstic equation is $Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$

Assessment

1. The output Q_n of a JK flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n and K_n are respectively

   a) 1,X b)0,X c)X,1 d) 0,1

2. When both the inputs of J-K flip-flop cycle are high, the output will -

   a) Invalid b)Change c)Toggle d) No Change


Thank
you