DIGITAL ELECTRONICS:
SYNCHRONOUS UP COUNTERS

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SYNCHRONOUS UP COUNTERS

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SYNCHRONOUS UP COUNTERS

- ✓ A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred.
- ✓ Counters are implemented using Flipflops.
- ✓ In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.

SYNCHRONOUS UP COUNTERS

APPLICATIONS

- ✓ Machine Motion control
- ✓ Motor RPM counter
- ✓ Rotary Shaft Encoders
- ✓ Digital clock or pulse generators.
- ✓ Digital Watch and Alarm systems.

DESIGN PROCEDURE

- ✓ **Step 1:** Select the required number of flipflops and the type of flipflops.
- ✓ **Step 2:** Draw the excitation table for the Flipflop.
- ✓ **Step 3:** Draw the state diagram.
- ✓ **Step 4:** Draw the excitation table for the logic diagram.
- ✓ **Step 5:** Draw K Map to find the minimal Boolean expression.
- ✓ **Step 6:** Draw the logic diagram for the up counter.

Problem Statement

Design a Synchronous 3 bit Up Counter

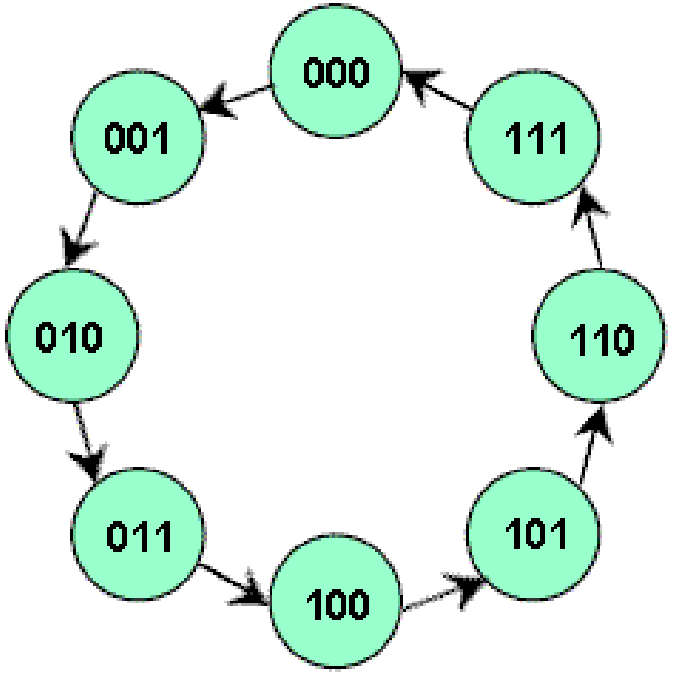
Step 1 :Select the required number of flipflops and the type of flipflops.

- Let us consider JK Flip Flop
- Since it is a 3 bit counter we need 3 flip flops.

Step 2: Draw the excitation table for the Flipflop.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	0
1	0	X	1
1	1	X	0

Step 3: Draw the state diagram



Step 4: Draw the excitation table for the logic diagram

Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	1	0	1	X	0	0	X	1	X
6	1	0	1	1	1	0	X	0	1	X	X	1
7	1	1	0	1	1	1	X	0	X	0	1	X
8	1	1	1	0	0	0	X	1	X	1	X	1

Step 5: Draw K Map to find the minimal Boolean expression.

For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

For J_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_A = 1$

For K_A

Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

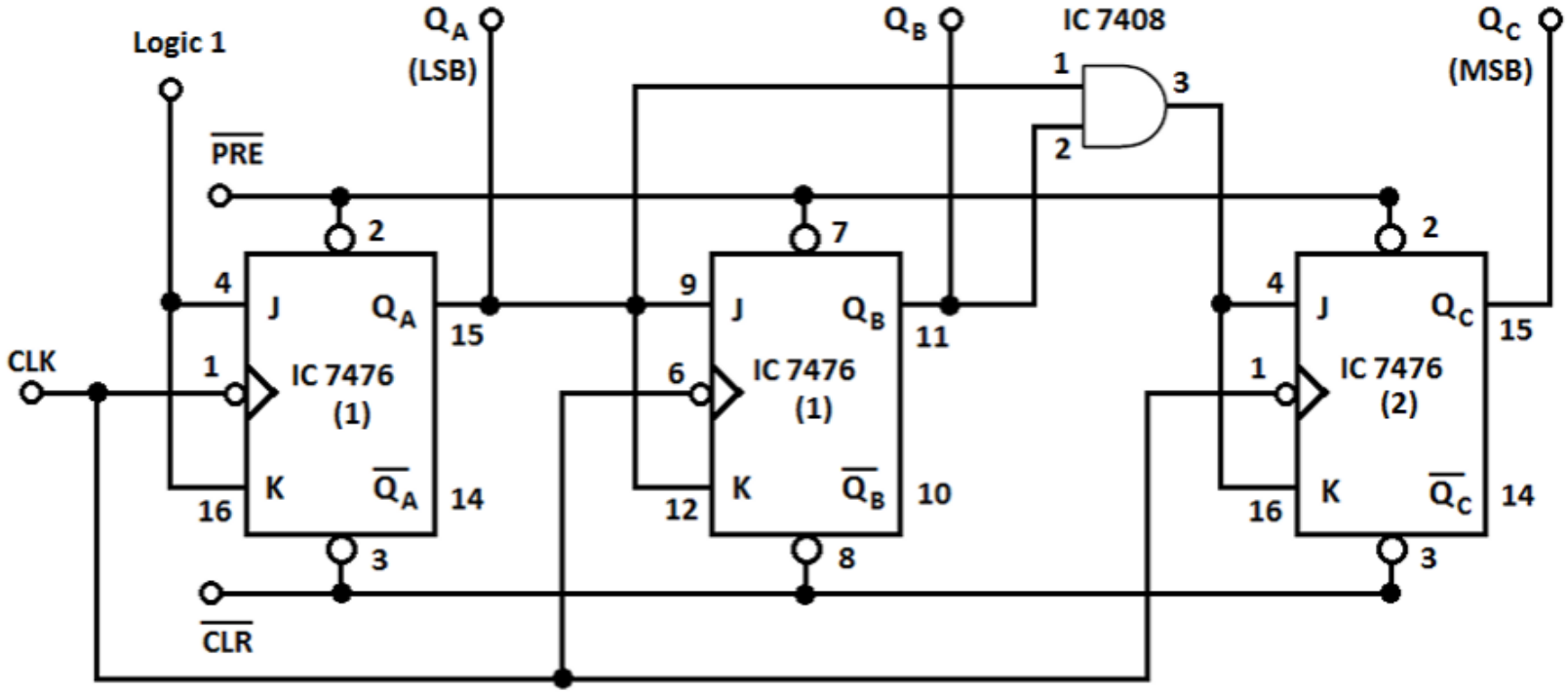
$K_A = 1$

Step 6: Draw the logic diagram for the up counter.

$J_A = 1$ $K_A = 1$

$J_B = Q_A$ $K_B = Q_A$

$J_C = Q_B Q_A$ $K_C = Q_B Q_A$



Assessment

1. How many Flipflops are required to design a 4 bit Counter?

2. How many states will be there for a 3 bit counter?


Thank
you