# DIGITAL ELECTRONICS:

## SYNCHRONOUS UP DOWN COUNTERS

# SNS COLLEGE OF ENGINEERING

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**An Autonomous Institution**

Accredited by NAAC – UGC with 'A' Grade

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## DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

## SYNCHRONOUS UP DOWN COUNTERS

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# SYNCHRONOUS UP DOWN COUNTERS

- ✓ A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred.
- ✓ Counters are implemented using Flipflops.
- ✓ In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.

# SYNCHRONOUS UP DOWN COUNTERS

## APPLICATIONS

- ✓ Microprocessors
- ✓ Timers
- ✓ Digital clock or pulse generators.
- ✓ Frequency dividers

# DESIGN PROCEDURE

- ✓ **Step 1:** Select the required number of flipflops and the type of flipflops.
- ✓ **Step 2:** Draw the excitation table for the Flipflop.
- ✓ **Step 3:** Draw the state diagram.
- ✓ **Step 4:** Draw the excitation table for the logic diagram.
- ✓ **Step 5:** Draw K Map to find the minimal Boolean expression.
- ✓ **Step 6:** Draw the logic diagram for the up Down counter.

# Problem Statement

Design a Synchronous 3 bit Up Down Counter

# Step 1 :Select the required number of flipflops and the type of flipflops.

- To perform 3 bit Up Down counting, 3 Flip Flops are required, which can count up to $2^3$-1 = 7.

- Here T Flip Flop is used.

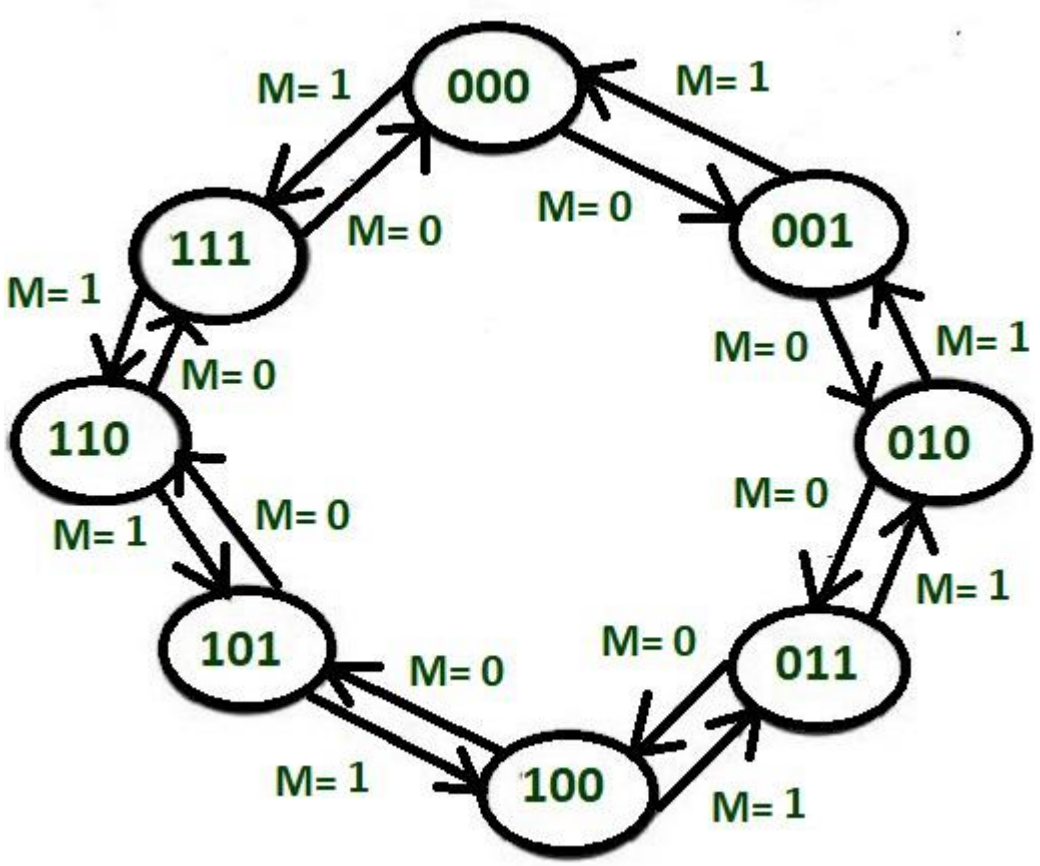
# Step 2: Draw the excitation table for the Flipflop.

| Previous state( $Q_n$ ) | Next state( $Q_{n+1}$ ) | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Step 3: Draw the state diagram

**Mode control input M**

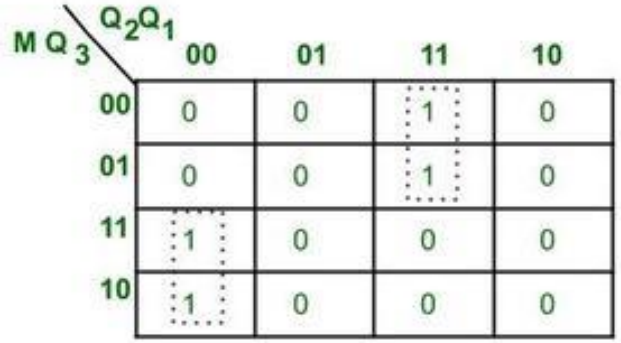
**When M=0 ,then the counter will perform up counting.**
**When M=1 ,then the counter will perform down counting.**



# Step 4: Draw the excitation table for the logic diagram

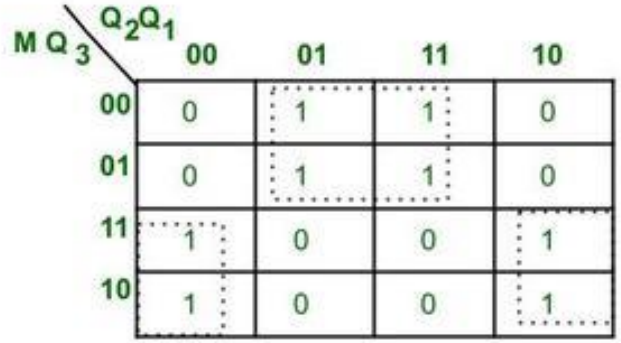
| M | $Q_3$ | $Q_2$ | $Q_1$ | $Q_3^*$ | $Q_2^*$ | $Q_1^*$ | $T_3$ | $T_2$ | $T_1$ |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

# Step 5: Draw K Map to find the minimal Boolean expression.



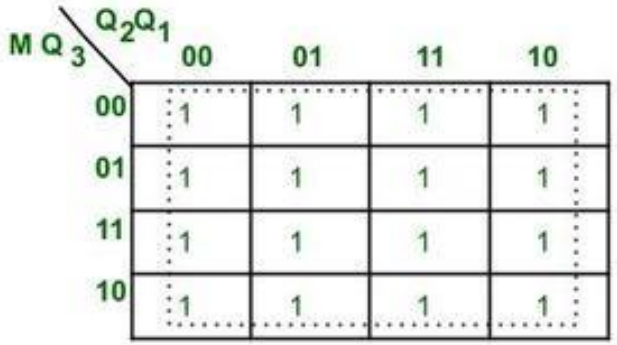
| $MQ_3$ \ $Q_2Q_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 1 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 0 |

$T_3 = M'Q_2Q_1 + MQ'_2\,Q'_1$



| $MQ_3$ \ $Q_2Q_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 0 | 1 |

$T_2 = M'Q_1 + MQ'_1$



| $MQ_3$ \ $Q_2Q_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

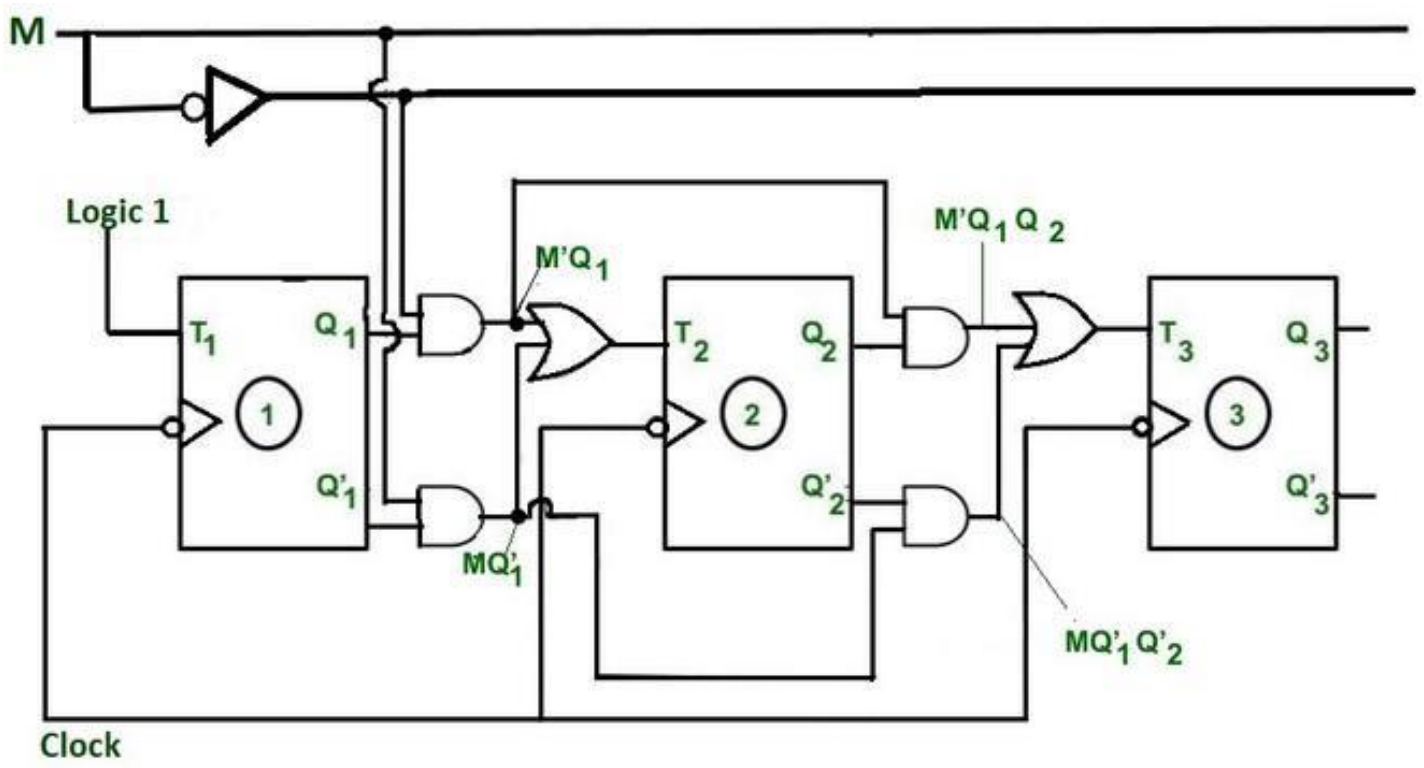
$T_1 = 1$

# Step 6: Draw the logic diagram for the up down counter.

$T_3 = M'Q_2Q_1 + MQ'_2\,Q'_1$

$T_2 = M'Q_1 + MQ'_1$

$T_1 = 1$



# Assessment

1. How many Flipflops are required to design a 4 bit Counter?

2. How many states will be there for a 3 bit counter?


Thank
you