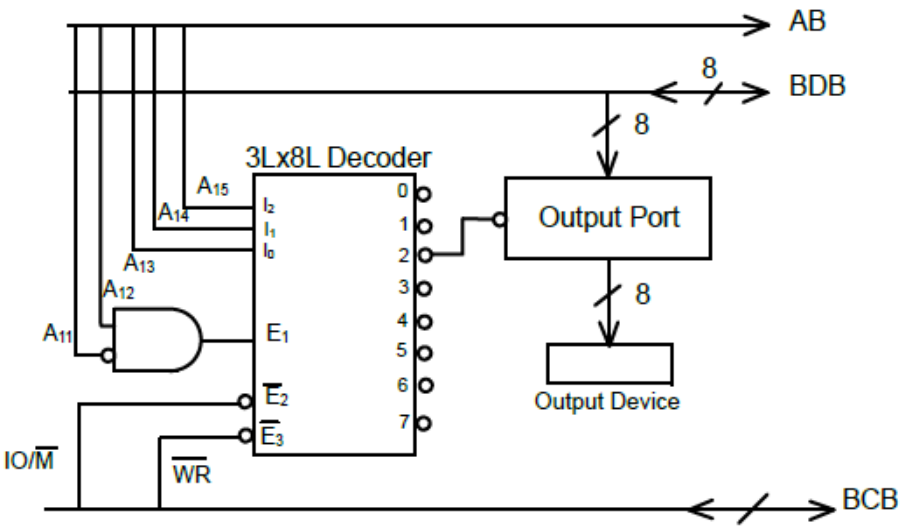
An output device is interfaced with 8-bit microprocessor 8085A. The interfacing circuit is shown in Figure (Gate 2014 SET 1)



The interfacing circuit makes use of 3 Line to 8 Line decoder having 3 enable lines $E_1, \overline{E_2}, \overline{E_3}$. The address of the device is

(A) 50 H (B) 5000 H (C) A0 H (D) A000 H

2. In an 8085 microprocessor, the following program is executed (Gate 2014 SET 2)
Address location – Instruction
2000H XRA A
2001H MVI B,04H
2003H MVI A, 03H
2005H RAR
2006H DCR B
2007H JNZ 2005
200AH HLT
At the end of program, register A contains

(A) 60H (B) 30H (C) 06H (D) 03H

In 8085A microprocessor, the operation performed by the instruction LHLD 2100H is

(A) (*H*)←21 *H* , (*L*)←00 *H*

(B) (*H*) ←*M* (2100 *H*) , (*L*) ←*M* (2101 *H*)

(C) (*H*) ←*M* (2101 *H*) , (*L*) ←*M* (2100 *H*)

(D) (*H*)←00 *H* , (*L*)←21 *H*

3.GATE 2011

A portion of the main program to call a subroutine SUB in an 8085 environment is given below.

```
        :
        :
        LXI   D, DISP
LP:     CALL  SUB
        :
        :
```

It is desired that control be returned to LP + DISP + 3 when the RET instruction is executed in the subroutine. The set of instructions that precede the RET instruction in the subroutine are

(A)
```
POP  D
DAD  H
PUSH D
```

(B)
```
POP  H
DAD  D
INX  H
INX  H
INX  H
PUSH H
```

(C)
```
POP  H
DAD  D
PUSH H
```

(D)
```
XTHL
INX  D
INX  D
INX  D
XTHL
```

4. Gate 2010

When a "**CALL** *Addr*" instruction is executed, the CPU carries out the following sequential operations internally:

Note:
(R) means content of register R
((R)) means content of memory location pointed to by R
PC means Program Counter
SP means Stack Pointer

(A) (SP) incremented
$(PC) \leftarrow Addr$
$((SP)) \leftarrow (PC)$

(B) $(PC) \leftarrow Addr$
$((SP)) \leftarrow (PC)$
(SP) incremented

(C) $(PC) \leftarrow Addr$
(SP) incremented
$((SP)) \leftarrow (PC)$

(D) $((SP)) \leftarrow (PC)$
(SP) incremented
$(PC) \leftarrow Addr$

5 Gate 2009

In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become

```
XRA A
MVIB F0H
SUB B
```

(A) 01 H (B) 0F H (C) F0 H (D) 10 H

6. Gate 2008

An input device is interfaced with Intel 8085A microprocessor as memory mapped I/O. The address of the device is 2500H. In order to input data from the device to accumulator, the sequence of instructions will be

(A)
```
LXI  H, 2500H
MOV  A, M
```
(B)
```
LXI  H, 2500H
MOV  M, A
```
(C)
```
LHLD 2500H
MOV  A, M
```
(D)
```
LHLD 2500H
MOV  M, A
```

7. Gate 2007

Which one of the following statements regarding the INT (interrupt) and the BRQ (bus request) pins in a CPU is true?

(A) The BRQ pin is sampled after every instruction cycle, but the INT is sampled after every machine cycle
(B) Both INT and BRQ are sampled after every machine cycle
(C) The INT pin is sampled after every instruction cycle, but the BRQ is sampled after every machine cycle
(D) Both INT and BRQ are sampled after every instruction cycle

8. Gate 2006

A software delay subroutine is written as given below:

```
DELAY:  MVI   H,   255 D
        MVI   L,   255 D
LOOP:   DCR   L
        JNZ   LOOP
        DCR   H
        JNZ   LOOP
```

How many times DCR L instruction will be executed ?

(*a*) 255
(*b*) 510
(*c*) 65025
(*d*) 65279

9 Gate 2006

In an 8085 A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D,E) register pair and store the result in same location. The sequence of instructions is

(*a*) XCHG
INR M

(*b*) XCHG
INX H

(*c*) INX D
XCHG

(*d*) INR M
XCHG

10.Gate 2004

If the following program is executed in a microprocessor, the number of instruction cycles it will take from START TO HALT is

```
START MV1A, 14 H    Move 14 H to register A

SHIFT RLC           Rotate left without carry

JNZ SHIFT           Jump on non-zero to SHIFT

HALT
```

(a) 4 (b) 8 (c) 13 (d) 16

11.Gate 2003

A memory system has a total of 8 memory chips, each with 12 address lines and 4 data lines. The total size of the memory system is

(a) 6 kbytes (b) 32 kbytes (c) 48 kbytes (d) 64 kbytes

12. Gate 2003

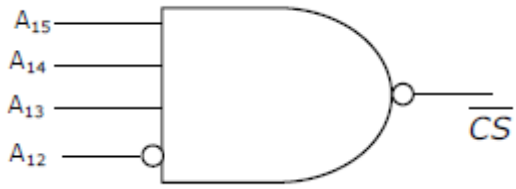
The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

```
LXI H, 1FFE
MOV B, M
INR L
MOV A, M
ADD B
INR L
MOV M, A
```

XOR A
On completion of the execution of the program, the result of addition is found
(a) in the register A (b) at the memory address 1000
(c) at the memory address 1F00 (d) at the memory address 2000

13 Gate 2002

The logic circuit used to generate the active low chip select (CS) by an 8085 microprocessor to address a peripheral is shown in Fig.1.14. The peripheral will respond to addresses in the range.
(a) E000-EFFF
(b) 000E-FFFE
(c) 1000-FFFF
(d) 0001-FFF1



14 gate 2001

An Intel 8085 processor is executing the program given below.
MVI A, 10H
MVI B, 10H
BACK: NOP
ADD B
RLC
JNC BACK
HLT
The number of times that the operation NOP will be executed is equal to
(a) 1 (b) 2 (c) 3 (d) 4

15. Gate 2000

Which one of the following is not a vectored interrupt?
(a) TRAP (b) INTR (c) RST7.5 (d) RST3

16.Gate 1997

In a microprocessor, the address of the next instruction to be executed, is stored in
(a) stack pointer
(b) address latch
(c) program counter
(d) general purpose register

17.Gate 1996

3.4. In a 8085 microprocessor, the following instructions may result in change of accumulator contents and change in status flags. Choose the correct match for each instruction.

		Contents of ACC	Cy flag	AC flag
(a) ANA r	(P)	unchanged	may by SET	unchanged
(b) XRA r	(Q)	unchanged	SET	SET
(c) CMP r	(R)	unchanged	SET	RESET
	(S)	may change	RESET	RESET
	(T)	may change	RESET	SET

18. Gate 1995

In an 8085 microprocessor, after the execution of XRA A instruction
(a) the carry flag is set (b) the accumulator contains $_{H}$FF
(c) the zero flag is set
(d) the accumulator contents are shifted left by one bit

19 gate 1995

A subroutine PROG1 written in the 8085 assembly language is given below. At entry to this program, the values of different registers in HEX are A = 05; BC = 0000; DE = 5472; HL = 4528. All the flags are set to 1. determine the register contents and condition of the zero and carry flags after the execution of the program. (i.e., after executing RET statement). What does the program accomplish?

```
PROG1 MOV A, E
ADD L
DAA
MOV L, A
MOV A, D
ADC H
DAA
MOV H, A

MVI A, 00H
RAL
RET
```

20. gate 1994

The contents of the accumulator in an 8085 microprocessor is altered after the execution of the instruction.

(*a*) CMPC (*b*) CPI 3 A

(*c*) ANI 5 C (*d*) ORA A

21. gate 1993

Three devices A, B and C have to be connected to a 8085 microprocessor. Device A has highest priority and device C has the lowest priority. In this context which of the following is correct assignment of interrupt inputs ?

(*a*) *A* uses TRAP, *B* uses RST 5.5 and C uses RST 6.5

(*b*) *A* uses RST 7.5, *B* uses RST 6.5 and C uses RST 5.5

(*c*) *A* uses RST 5.5, *B* uses RST 6.5 and C uses RST 7.5

(*d*) *A* uses RST 5.5, *B* uses RST 6.5 and C uses TRAP