SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE AND DESIGN

COURSE NAME : 19EE01 BASIC ELECTRICAL AND ELECTRONICS ENGINEERING

I YEAR /II SEMESTER - COMPUTER SCIENCE AND DESIGN

Topic 6 : Half Adder

Design procedure – Half adder

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM and CARRY. The SUM output is the least significant bit (LSB) of the result, while the CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The half adder can be implemented using basic gates such as XOR and AND gates.

Sure, here's a more in-depth explanation of the half adder circuit:
The half adder is a basic building block for more complex adder circuits such as full adders and multiple-bit adders. It performs binary addition of two single-bit inputs, A and B, and provides two outputs, SUM and CARRY.
The SUM output is the least significant bit (LSB) of the result, which is the XOR of the two inputs A and B. The XOR gate implements the addition operation for binary digits, where a "1" is generated in the SUM output only when one of the inputs is "1".
The CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The CARRY output is the AND of the two inputs A and B. The AND gate generates a "1" in the CARRY output only when both inputs are "1".

Half Adder (HA):

Half adder is the simplest of all adder circuits. Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (s) and carry bit (c) both as output. The addition of 2 bits is done using a combination circuit called a Half adder. The input variables are augend and addend bits and output variables are sum & carry bits. A and B are the two input bits.

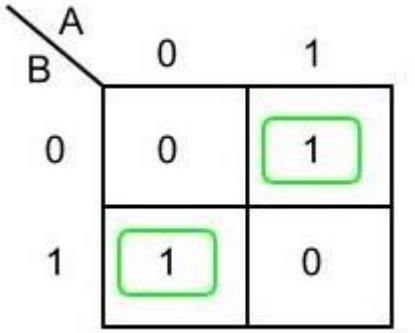
let us consider two input bits A and B, then sum bit (s) is the X-OR of A and B. it is evident from the function of a half adder that it requires one X-OR gate and one AND gate for its construction.

Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

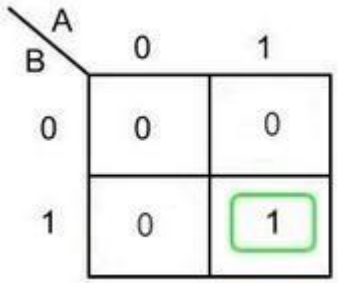
Logical Expression:

For Sum:



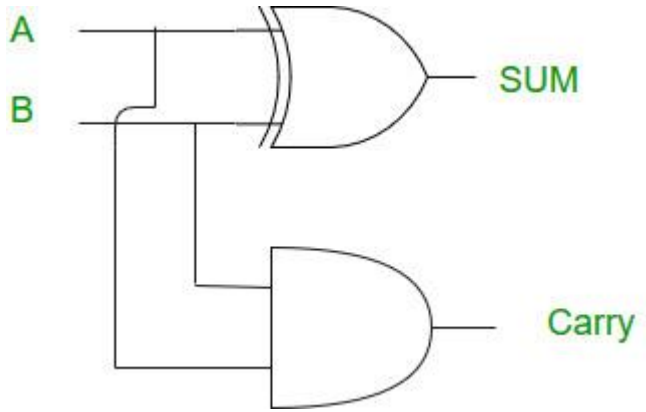
Sum = A XOR B

For Carry:



Carry = A AND B

Implementation:



Note: Half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multi addition is performed.

Advantages and disadvantages of Half Adder in Digital Logic :

Advantages of Half Adder in Digital Logic :

Simplicity, Speed

Disadvantages of Half Adder in Digital Logic :

Limited Usefulness, Lack of Convey Info, Propagation Deferral

Application of Half Adder in Digital Logic

Arithmetic circuits, Data handling, Address unraveling, Encoder and decoder circuits, Multiplexers and demultiplexers, Counters

Any Query????

Thank you……