DC Characteristics of Op-Amp

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal DC characteristics that add error components to the DC output voltage are:

(i) Input bias current

(ii)Input offset current

(iii) Input offset voltage

(iv) Thermal drift.

Input Bias Current

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying currents into the bases by the external circuit. In an ideal op-amp, we assume that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of DC current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as I_B^- and I_B^+ respectively in Fig. 1 (a). Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs. Manufacturers specify input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

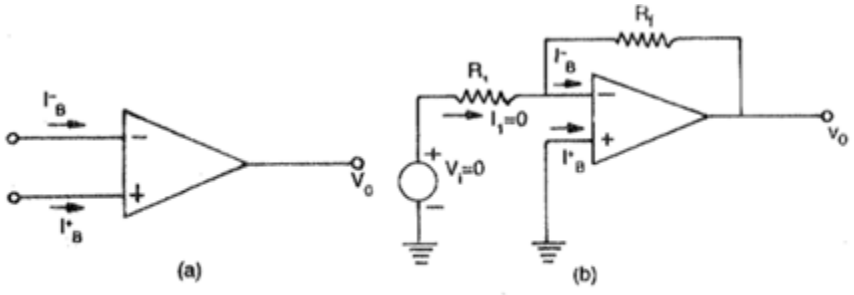

Fig. 1 (a) Input bias currents (b) inverting amplifier with bias currents

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

For 741, a bipolar op-amp, the bias current is 500 nA or less. The FET input op-amp will have bias currents as low as 50 pA at room temperature.

Consider the basic inverting amplifier of Fig. 1 (b). If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$V_o = (I_B^-)R_f$$

For a 741 op-amp, with a 1 MΩ feedback resistor,

$$V_o = 500 \text{ nA} \times \text{I MΩ} = 500 \text{ mV}$$

The output is driven to 500 mV with zero input because of the bias currents. In applications where signal levels are measured in millivolts, this is totally unacceptable. This effect can be compensated for as shown in Fig. .1 (c) where a compensation resistor R_{comp} has been added between the noninverting input terminal and ground. Current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then, by KVL, we get,

$$-V_1 + 0 + V_2 - V_o = 0$$

or

$$V_o = V_2 - V_1 \quad (1)$$

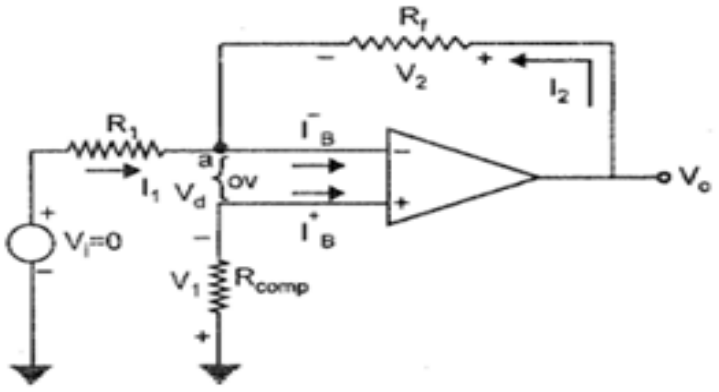

Fig. 1 (c) Bias current compensation

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. The value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

or
$$I_B^+ = \frac{V_1}{R_{comp}} \qquad (2)$$

The node 'a' is at voltage $(-V_1)$, because the voltage at the non-inverting input terminal is $(-V_1)$. So, with $V_i = 0$, we get,

$$I_1 = \frac{V_1}{R_1}$$

Also,
$$I_2 = \frac{V_2}{R_f}$$

For compensation, V_o should be zero for $V_i = 0$, that is, from Eq. (1) $V_2 = V_1$

So that,
$$I_2 = \frac{V_1}{R_f}$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_f)}{R_1 R_f} \qquad (3\ )$$

Assuming $I_B^- = I_B^+$ and using Eqs. (2) and (3) we get,

$$V_1 \frac{(R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

or,
$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \parallel R_f \qquad (4)$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

Input Offset Current

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^-$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero. Referring to Fig. 1 (c),

$$V_1 = I_B^+ R_{comp}$$

and

$$I_1 = \frac{V_1}{R_1}$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1}\right)$$

Again

$$V_o = I_2 R_f - V_1$$

$$= I_2 R_f - I_B^+ R_{comp}$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp}$$

Substituting Eq. (4) and after algebraic manipulation,

$$V_o = R_f [I_B^- - I_B^+]$$

So,

$$V_o = R_f I_{os} \qquad (5)$$

So even with bias current compensation and with the feedback resistor of 1 MΩ, a 741 BJT op-amp has an output offset voltage

$$V_o = 1\ \text{M}\Omega \times 200\ \text{nA} = 200\ \text{mV}$$

with a zero input voltage. It can be seen from Eq. (5) that the effect of offset current can be minimized by keeping feedback resistance small. Unfortunately, to obtain high input impedance, R_1 must be kept large. With R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

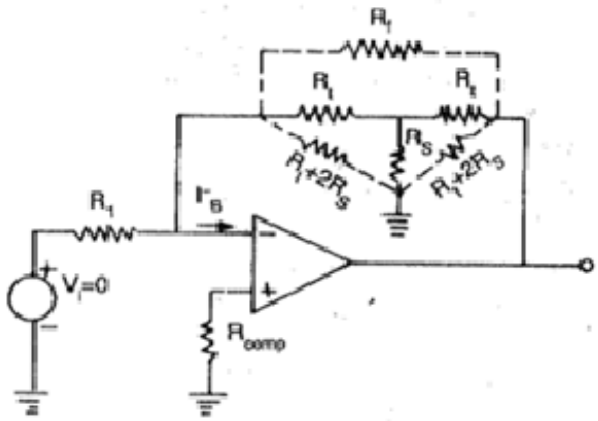

Fig. 1 (d) Inverting amplifier with T-feedback network

The T-feedback network in Fig. 1 (d) is a good solution. This will allow large feedback resistance, while keeping the resistance to ground (seen by the inverting input) low as shown in the dotted network. The T-network provides a feedback signal as if the network were a single feedback resistor. By T to π conversion,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design a T-network, first pick

$$R_t << \frac{R_f}{2}$$

Then calculate $R_s = \dfrac{R_t^2}{R_f - 2R_t}$

Input Offset Voltage

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in Fig. 2. (a).

Let us now examine the effect of V_{os} on the output of a non-inverting and inverting op-amp amplifier as shown in Fig. 2 (b, c). If V_i is set to zero, the circuits of Fig. 2 (b and c) become the same as in Fig. 2 (d). The voltage V_2 at the (–) input terminal is given by

$$V_2 = \left(\frac{R_1}{R_1 + R_f}\right)V_o$$

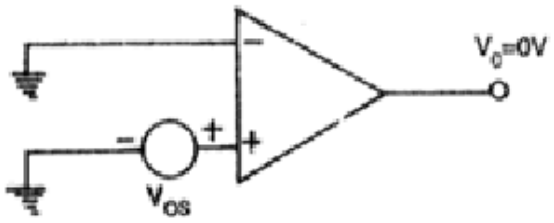

Fig. .2 (a) Op-amp showing input offset voltage

or $$V_o = \left(\frac{R_1 + R_f}{R_1}\right) V_2 = \left(1 + \frac{R_f}{R_1}\right) V_2$$

Since, $$V_{os} = |V_i - V_2| \text{ and } V_i = 0,$$

$$V_{os} = |0 - V_2| = V_2$$

or, $$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{os} \qquad (6)$$

Thus, the output offset voltage of an op-amp in closed-loop configuration (inverting or non-inverting) is given by Eq (6)

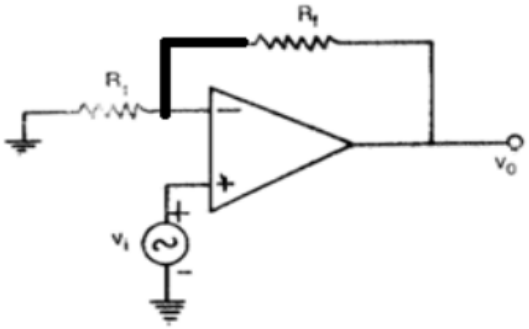

Fig. .2 (b) Non-inverting amplifier

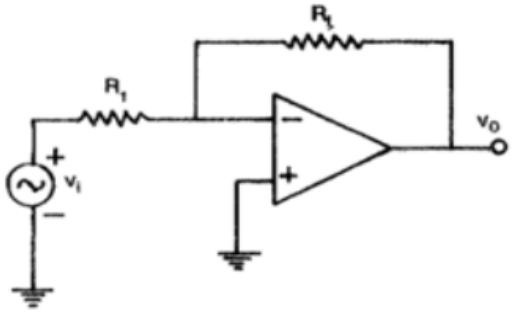

Fig. .2 (c) Inverting amplifier

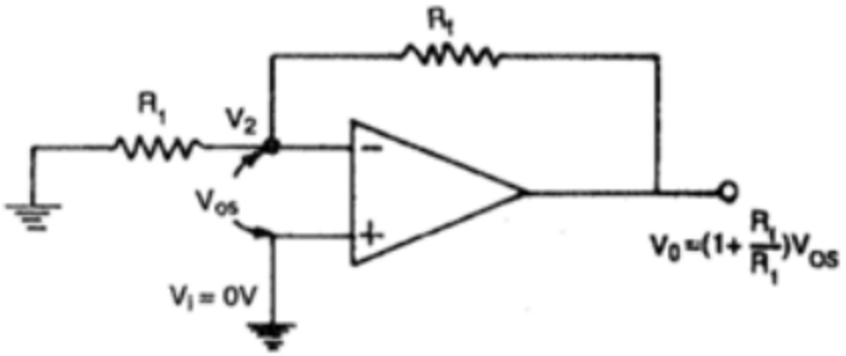

Fig. 2 (d) equivalent circuit for $V_i = 0$

Thermal Drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.