PROBLEMS

Problem 1

Design an amplifier with a gain of –10 and input resistance equal to 10 kΩ.

Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

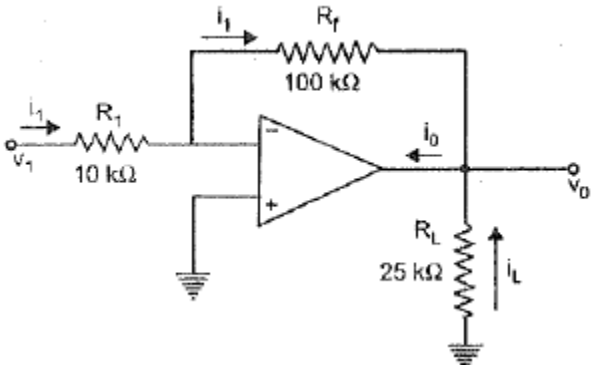
In Fig. 2.5 (a) choose $R_1 = 10\ \text{k}\Omega$

Then $R_f = -A_{CL} R_1$ (from Eq. 2.4)

$= -(-10) \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$

Problem 2

In Fig. 2.5 (b), $R_1 = 10\ \text{k}\Omega$, $R_f = 100\ \text{k}\Omega$, $v_i = 1\ V$. A load of 25 kΩ is connected to the output terminal. Calculate (i) i_1 (ii) v_o (iii) i_L and total current i_o into the output pin.



Solution

(a) $i_1 = \dfrac{v_i}{R_1} = \dfrac{1V}{10\ \text{k}\Omega} = 0.1\ \text{mA}$

(b) $v_o = -\dfrac{R_f}{R_1} v_i = -\dfrac{100\ \text{k}\Omega}{10\ \text{k}\Omega} 1V = -10V$

(c) $i_L = \dfrac{v_o}{R_L} = \dfrac{10\ V}{25\ \text{k}\Omega} = 0.4\ \text{mA}$

The direction of i_L is shown in Fig. 2.5 (b).

(d) i_1 as calculated above is 0.1 mA.

Therefore, total current $i_o = i_1 + i_L = 0.1\ \text{mA} + 0.4\ \text{mA} = 0.5\ \text{mA}$. In an inverting amplifier, for a + ive input, output will be –ive, therefore the direction of i_o is as shown in Fig. 2.5 (b).

Problem 3

Design an amplifier with a gain of +5 using one op-amp.

Solution

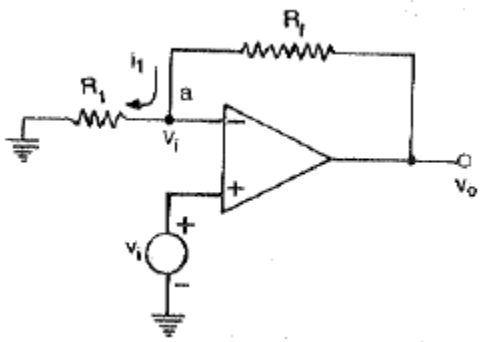
Since the gain is positive, we have to make a non-inverting amplifier.

In Fig. select $R_1 = 10\ \text{k}\Omega$. Then

$$A_{CL} = 1 + R_f/R_1$$

or, $$5 = 1 + R_f/10\ \text{k}\Omega$$

or, $$R_f = 4 \times 10\ \text{k}\Omega = 40\ \text{k}\Omega$$



Problem 4

(a) For the non-inverting amplifier of Fig. 3.2 (b), $R_1 = 1\ \text{k}\Omega$ and $R_f = 10\ \text{k}\Omega$. Calculate the maximum output offset voltage due to V_{os} and I_B. The op-amp is LM 307 with $V_{os} = 10$ mV and $I_B = 300$ nA, $I_{os} = 50$ nA.

(b) Calculate the value of R_{comp} needed to reduce the effect of I_B.

(c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

Solution

(a) $$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

$$= \left(1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega}\right) (10\ \text{mV}) + (10\ \text{k}\Omega)\ (300\ \text{nA})$$

$$= 110\ \text{mV} + 3\ \text{mV} = 113\ \text{mV}$$

(b) The value of R_{comp} needed is,

$$R_{comp} = 1\ \text{k}\Omega \,||\, 10\ \text{k}\Omega = 990\ \Omega$$

(c) With R_{comp} in the circuit,

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$$

$$= 110\ \text{mV} + 0.5\ \text{mV} = 110.5\ \text{mV}$$

Problem 5

A non-inverting amplifier with a gain of 100 is nulled at 25°C. What will happen to the output voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C ?

Solution

Input offset voltage due to temperature rise = 0.15 mV/°C × (50°C − 25°C) = 3.75 mV. Since this is an input change, the output voltage will change by

$$V_o = V_{os} \times A_{CL}$$

$$= 3.75\ \text{mV} \times 100 = 375\ \text{mV}$$

This could represent a very major shift in the output voltage.

Problem 6

Design an adder circuit using an op-amp to get the output expression as

$$V_o = -(0.1\ V_1 + V_2 + 10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

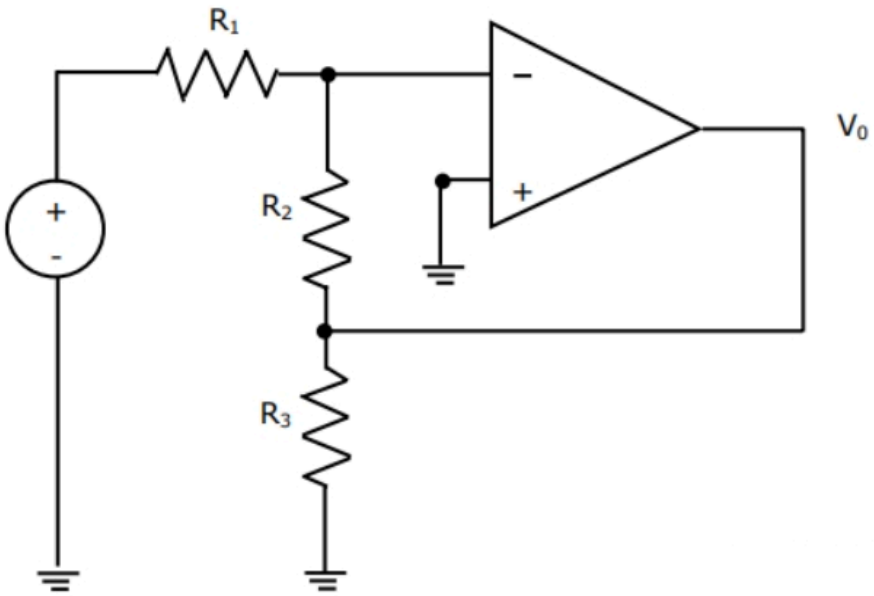
$$V_o = -[(R_f/R_1)\ V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$

say $R_f = 10\ \text{k}\Omega,\ R_1 = 100\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_3 = 1\ \text{k}\Omega$

Then the desired output expression is obtained.

Problem 7[GATE EC 2010]

Assuming the OP-AMP to be ideal, the voltage gain of the amplifier shown below is

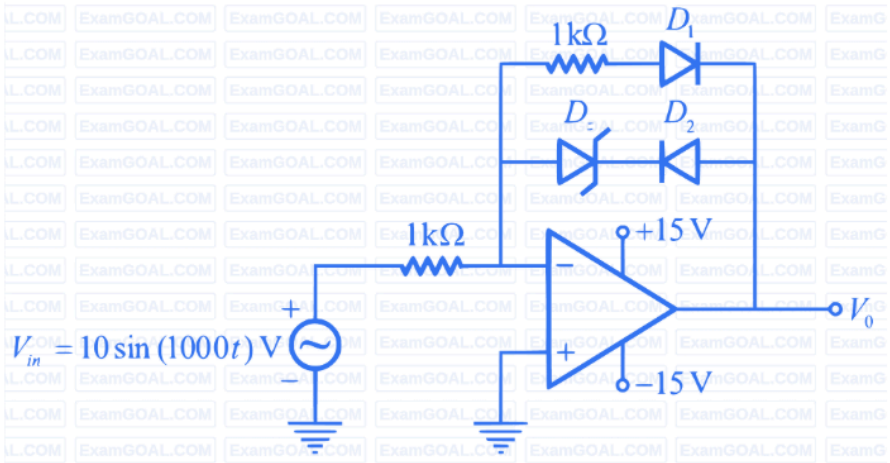


Correct Answer

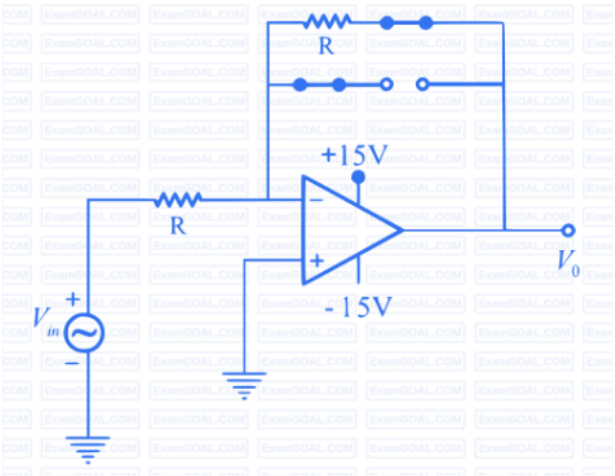
A $-\frac{R_2}{R_1}$

Problem 8 [GATE EE 2023]

Consider the OP AMP based circuit shown in the figure. Ignore the conduction drops of diodes D_1 and D_2. All the components are ideal and the breakdown voltage of the Zener is 5 V. Which of the following statements is true?



For positive half cycle the diodes D_1 and D_z are forward bias and D_2 is reverse biased and the circuit is shown below,

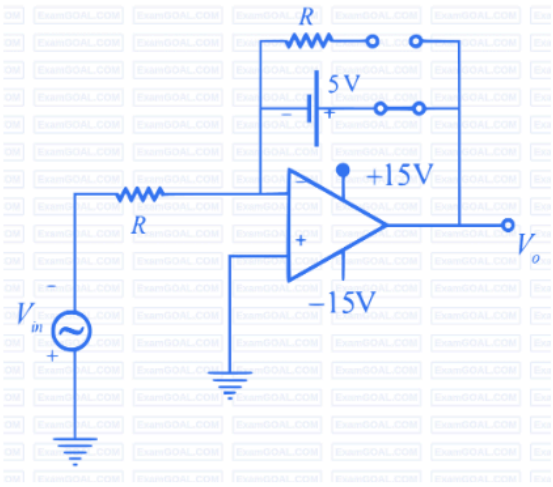


When $V_{\text{in}} = 10\ \text{V}$,

$V_0 = \frac{-R}{R} \times 10 = -10\ \text{V}$

$\therefore V_0$ will be -10 V .

For negative half cycle, diode D_2 is forward bias and D_1, D_z is reverse bias. Zener diode is in breakdown region and the circuit is shown below,



$\therefore V_0 = 5\ \text{V}$

$\Rightarrow V_{0_{\max}} = 5\ \text{V}$ and $V_{0_{\min}} = -10\ \text{V}$

Correct Answer

D The maximum and minimum values of the output voltage V_0 are +5 V and -10 V, respectively.