## **DIGITAL TO ANALOG CONVERTER (DAC)**

A **Digital to Analog Converter (DAC)** converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1.



A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the **number of binary inputs** of a DAC will be a power of two.

Types of DACs

There are **two types** of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

## WEIGHTED RESISTOR DAC

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

The circuit diagram of a 3-bit binary weighted resistor DAC is shown in the following figure -



Let the **3-bit binary input** is  $b_2 b_1 b_0$ . Here, the bits  $b_2$  and  $b_0$  denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively.

The **digital switches** shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage,  $-V_R$  when the corresponding input bits are equal to '1'.

In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

The **nodal equation** at the inverting input terminal's node is:

$$\begin{split} \frac{0+V_Rb_2}{2^0R} + \frac{0+V_Rb_1}{2^1R} + \frac{0+V_Rb_0}{2^2R} + \frac{0-V_0}{R_f} = 0 \\ = &> \frac{V_0}{R_f} = \frac{V_Rb_2}{2^0R} + \frac{V_Rb_1}{2^1R} + \frac{V_Rb_0}{2^2R} \\ = &> V_0 = \frac{V_RR_f}{R} \bigg\{ \frac{b_2}{2^0} + \frac{b_1}{2^1} + \frac{b_0}{2^2} \bigg\} \end{split}$$

Substituting,  $R = 2R_{ff}$  in above equation.

$$=>V_0=rac{V_RR_f}{2R_f}iggl\{rac{b_2}{2^0}+rac{b_1}{2^1}+rac{b_0}{2^2}iggr\} \ =>V_0=rac{V_R}{2}iggl\{rac{b_2}{2^0}+rac{b_1}{2^1}+rac{b_0}{2^2}iggr\}$$

The above equation represents the **output voltage equation** of a 3-bit binary weighted resistor DAC. Since the number of bits are three in the binary (digital) input, we will get seven possible values of output voltage by varying the binary input from 000 to 111 for a fixed reference voltage,  $V_R$ .

We can write the **generalized output voltage equation** of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$=>V_0=rac{V_R}{2}iggl\{rac{b_{N-1}}{2^0}+rac{b_{N-2}}{2^1}+\ldots+rac{b_0}{2^{N-1}}iggr\}$$

The disadvantages of a binary weighted resistor DAC are as follows -

- The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.
- It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

### **R-2R LADDER DAC**

The R-2R configuration is a simple arrangement that consists of parallel and series resistors connected in cascaded form to an operational amplifier. We can use an operational amplifier in inverting or non-inverting form, depending on the polarity of the output voltage that we want to get from the DAC. R-2R ladder resistors act as voltage dividers along with the entire network, with the output voltage dependent on the input voltages.

The circuit diagram of a 3-bit R-2R Ladder DAC is shown in the following figure –



The ladder arrangement consists of two resistors, i.e., a base resistor R and a 2R resistor, which is twice the value of the base resistor. This feature helps to maintain a precise output analog signal without using a wide range of resistor values. A pair of R and 2R is used for one input bit. The digital inputs are provided through binary switches connected to Vref for input 1 and GND for input 0.

# 3-bit R-2R Ladder DAC

Consider a 3-bit R-2R ladder DAC. The following diagram shows the R-2R 3-bit ladder DAC. The leftmost side of the circuitry has the least significant bit, i.e., B0, whereas B2, which is the most significant bit, connects to the amplifier. The binary inputs are given through the binary switches. So, when we need a high bit, simply connect the relevant bit to the reference voltage, and when we require a low bit, the switch connects to the ground potential.



Thevenin's theorem is a technique through which we can obtain an equivalent circuit of the concerned resistance network. A Thevenin circuit consists of a Thevenin resistance and a Thevenin voltage that we can replace in the circuit, and it still works the same as the original resistance network.



As we need a Thevenin resistance and a Thevenin voltage for substitution, we first calculate  $R_{Th}$  by short-circuiting all the voltage sources and replacing the current sources with open circuits.  $V_{TH}$  is the no-load output voltage and is entirely dependent on the position of the input switches. Now, replace the original circuit with the Thevenin circuit. Hence, we obtain the total output voltage of a 3-bit R-2R ladder network by considering only one high bit at a time and summing the individual voltages of each bit using superposition to obtain the transfer function of the DAC.

When LSB is high, let us first consider the binary code 001. Its  $V_{TH}$  and  $R_{TH}$  will be calculated in three stages.



The first stage measures the V<sub>Th</sub> and R<sub>Th</sub> of the dotted block. The dotted block is separately shown in the right figure. We can see that it is just a voltage divider circuit. So, Vth is calculated using the formula:  $V_{th} = [2R/(2R+2R)]*V_{ref} = V_{ref}/2$ 

#### First Equivalent Circuit

Below is the equivalent circuit of the original after simplifying the first stage. The Thevenin equivalent of the first stage is connected in series to the rest of the circuit.



Now, we calculate the Thevenin circuit of the second stage. We will solve the dotted block in the second stage. Two resistors of the same value, i.e., R, connect in series. So we replace them by the equivalent resistance 2R in the diagram below. The circuit is again configured to be a voltage divider with a reference voltage of Vref/2. So,  $V_{th} = [2R/(2R+2R)]*(V_{ref}/2) = V_{ref}/4$  and Rth = R

The second equivalent circuit is



This is the resultant circuit, which will be solved in the third stage. The VTh and RTh are as follows:  $V_{th} = [2R/(2R+2R)]*(V_{ref}/4) = V_{ref}/8$  and Rth = R



In general, the output voltage of R-2R ladder is

The advantages of a R-2R Ladder DAC are as follows -

- R-2R Ladder DAC contains only two values of resistor: R and 2R. So, it is easy to select and design more accurate resistors.
- If more number of bits are present in the digital input, then we have to include required number of R-2R sections additionally.

Due to the above advantages, R-2R Ladder DAC is preferable over binary weighted resistor DAC.