SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

555 Timer

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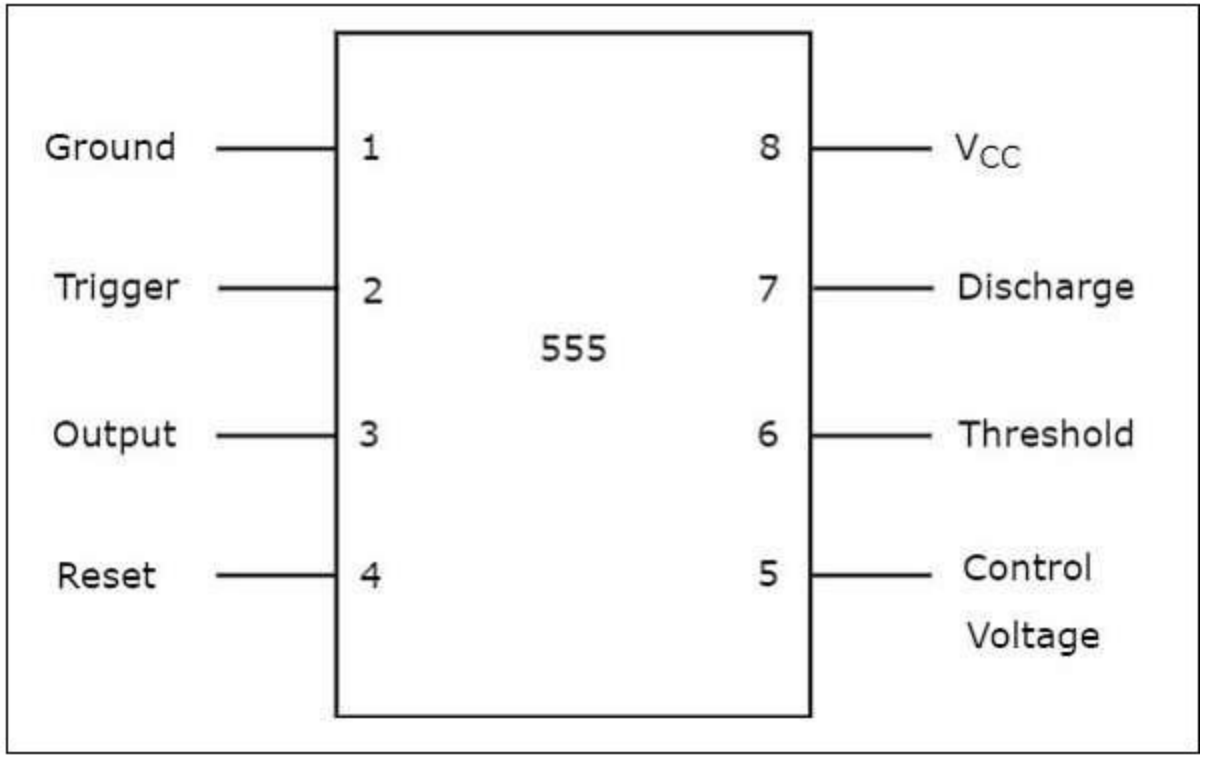
555 Timer

The **555 Timer** IC got its name from the three 5kΩ resistors that are used in its voltage divider network.

This IC is useful for generating accurate time delays and oscillations.

555 Timer IC

The 555 Timer IC is an 8 pin mini Dual-Inline Package (DIP)

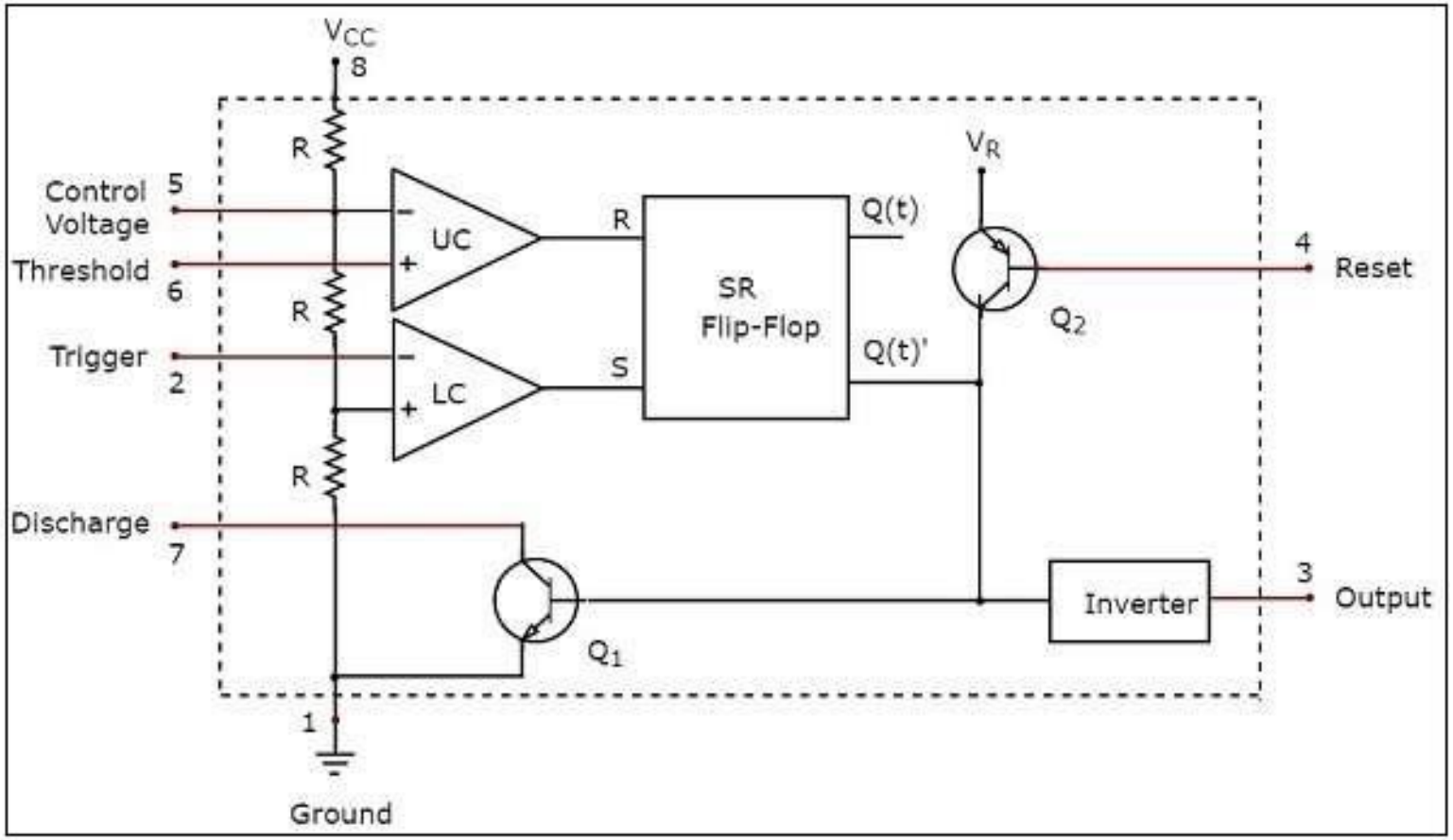


555 Timer

- ✔This 555 Timer IC can be operated with a DC supply of +5V to +18V.

- ✔It is mainly useful for generating **non-sinusoidal** wave forms like square, ramp, pulse & etc

Functional Diagram



Functional Diagram

Functional diagram of 555 Timer contains:

- ✔ A voltage divider network
- ✔ Two comparators
- ✔ One SR flip-flop
- ✔ Two transistors
- ✔ An inverter

Voltage divider network

- The voltage divider network consists of a three 5kΩ resistors that are connected in series between the supply voltage V_{cc} and ground.

- This network provides a voltage of V_{cc3} between a point and ground, if there exists only one 5kΩresistor. Similarly, it provides a voltage of $2V_{cc3}$ between a point and ground, if there exists only two 5kΩ resistors.

Comparators

- The functional diagram of a 555 Timer IC consists of two comparators: an Upper Comparator (UC) and a Lower Comparator (LC).

- **Comparator** compares the two inputs that are applied to it and produces an output.

- If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be $+V_{sat}$. This can be considered as **Logic High** ('1') in digital representation.

- If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be $-V_{sat}$. This can be considered as **Logic Low** ('0') in digital representation.

SR Flip Flop

- Recall that a **SR flip-flop** operates with either positive clock transitions or negative clock transitions.

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	-

- It has two inputs: S and R, and two outputs: Q(t) and Q(t)' which are complement to each other.
- Here, Q(t) & Q(t+1) are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive (negative) transition of clock signal is applied.
- The outputs of Lower Comparator (LC) and Upper Comparator (UC) are applied as **inputs of SR flip-flop**

Transistors and Inverter

- The functional diagram of a 555 Timer IC consists of one npn transistor Q1 and one pnp transistor Q2.

- The npn transistor Q1 will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.

- The pnp transistor Q2 is used as **buffer** in order to isolate the reset input from SR flip-flop and npn transistor Q1.

- The **inverter** used in the functional diagram of a 555 Timer IC not only performs the inverting action but also amplifies the power level.

Applications

- ✔The 555 Timer IC can be used in mono stable operation in order to produce a pulse at the output.
- ✔Similarly, it can be used in astable operation in order to produce a square wave at the output.

Assessment

1. List the major components of 555 Timer.

2. What will be the output of 555 Timer under astable operation.


Thank
you